

AD-A130 145 REVERSE BIAS SECOND BREAKDOWN IN POWER SWITCHING
TRANSISTORS(U) TEXAS TECH UNIV LUBBOCK W M PORTNOY
MAY 83 AFWL-TR-82-139 F29601-81-K-0037

REVERSE BIAS SECOND BREAKDOWN IN POWER SWITCHING
TRANSISTORS(U) TEXAS TECH UNIV LUBBOCK W M PORTNOY
MAY 83 AFWL-TR-82-139 F29601-81-K-0037

1 / 1

UNCLASSIFIED F/G 9/1

F/G 9/1

NL

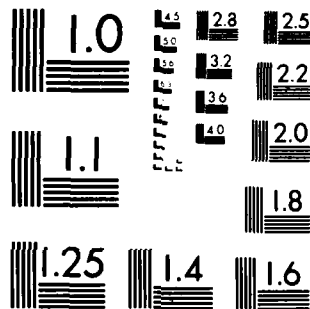
END

D611

FILMED

8 83

DTIC



MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS 1963-A

AD A130145

REVERSE BIAS SECOND BREAKDOWN IN POWER
SWITCHING TRANSISTORS

W. M. Portnoy

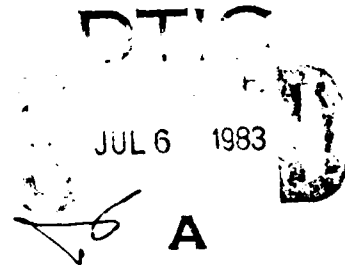
Texas Tech University
Lubbock, Texas 79409

May 1983

Final Report

Approved for public release; distribution unlimited.

AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117



DTIC FILE COPY

83 07 6 033

This final report was prepared by the Texas Tech University, Lubbock, Texas, under Contract F29601-81-K-0037, Job Order 37630148 with the Air Force Weapons Laboratory, Kirtland Air Force Base, New Mexico. Mark E. Snyder (NTAT) was the Laboratory Project Officer-in-Charge.

When Government drawings, specifications, or other data are used for any purpose other than in connection with a definitely Government-related procurement, the United States Government incurs no responsibility or any obligation whatsoever. The fact that the Government may have formulated or in any way supplied the said drawings, specifications, or other data, is not to be regarded by implication, or otherwise in any manner construed, as licensing the holder, or any other person or corporation; or as conveying any rights or permission to manufacture, use, or sell any patented invention that may in any way be related thereto.

This report has been authored by a contractor of the United States Government. Accordingly, the United States Government retains a nonexclusive, royalty-free license to publish or reproduce the material contained herein, or allow others to do so, for the United States Government purposes.

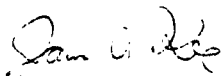
This report has been reviewed by the Public Affairs Office and is releasable to the National Technical Information Services (NTIS). At NTIS, it will be available to the general public, including foreign nations.

If your address has changed, if you wish to be removed from our mailing list, or if your organization no longer employs the addressee, please notify AFWL/NTAT, Kirtland AFB, NM 87117 to help us maintain a current mailing list.

This technical report has been reviewed and is approved for publication.

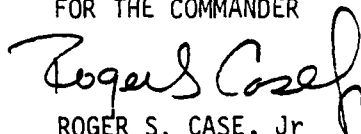


MARK E. SNYDER
2nd Lt, USAF
Project Officer



JAMES A. KEE
Maj, USAF
Chief, Technology Branch

FOR THE COMMANDER



ROGER S. CASE, Jr
Lt Col, USAF
Chief, Aircraft & Missile Division

DO NOT RETURN COPIES OF THIS REPORT UNLESS CONTRACTUAL OBLIGATIONS OR NOTICE ON A SPECIFIC DOCUMENT REQUIRES THAT IT BE RETURNED.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFWL-TR-82-139	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) REVERSE BIAS SECOND BREAKDOWN IN POWER SWITCHING TRANSISTORS	5. TYPE OF REPORT & PERIOD COVERED Final Report	
	6. PERFORMING ORG. REPORT NUMBER	
7. AUTHOR(s) W. M. Portnoy	8. CONTRACT OR GRANT NUMBER(s) F29601-81-K-0037	
9. PERFORMING ORGANIZATION NAME AND ADDRESS Texas Tech University Lubbock, Texas 79409	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 64711F/37630148	
11. CONTROLLING OFFICE NAME AND ADDRESS Air Force Weapons Laboratory (NTAT) Kirtland Air Force Base, NM 87117	12. REPORT DATE May 1983	
	13. NUMBER OF PAGES 60	
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)	15. SECURITY CLASS. (of this report) Unclassified	
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE	
16. DISTRIBUTION STATEMENT (of this Report) Approved for public release; distribution unlimited.		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Electrical Overstress Second Breakdown Transistors Switching		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) The second breakdown characteristics under reverse base drive have been investigated for two n-p-n power switching transistor structures using a non-destructive testing circuit. Three types of second breakdown have been identified, all occurring in a single device under different operating conditions. Primary mechanisms, neither of which involve a critical temperature, have been proposed for two of the types. The third type has not previously been reported, nor has a mechanism been proposed. The experimental evidence at this time excludes adiabatic heating as a principal cause of second breakdown in the test devices.		

DD FORM 1 JAN 73 1473

EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

TABLE OF CONTENTS

	Page
I. INTRODUCTION.	5
II. TESTER OPERATION.	7
GENERAL DESCRIPTION OF THE TESTER	7
DETAILS OF THE TEST SYSTEM.	7
CONSTRUCTION OF THE TESTER.	17
III. EXPERIMENTAL PROCEDURES AND RESULTS	25
MEASUREMENT SYSTEM.	25
TEST DEVICES.	25
TEST CONDITIONS	32
TYPES OF SECOND BREAKDOWN	32
EXPERIMENTAL RESULTS.	37
IV. CONCLUSIONS	58
LIST OF REFERENCES.	59



Approved For

A

LIST OF TABLES

Table		Page
1.	IDENTIFICATION OF UNITRODE TRANSISTORS BY LOT TYPES.	26
2.	MEASURED DEVICE PARAMETERS	33

LIST OF FIGURES

Figure	Page
1. Simplified schematic of the tester.	8
2. Block diagram of base drive circuit	9
3. Block diagram of the protection circuit	12
4. Detailed schematic diagram of the protection circuit.	13
5. Detailed schematic of protection circuit power supplies.	15
6. Schematic diagram of the collector voltage supply . .	16
7. Front chassis of the tester	18
8. Detailed schematic diagram of the base drive circuit.	19
9. Voltage regulator circuits for the base drive power supplies.	20
10. Back chassis of the tester.	22
11. Front part of the crowbar circuit	23
12. Back chassis with crowbar circuit folded down	24
13. A unitrode NE masked transistor magnified 9 times . .	27
14. A unitrode NH masked transistor magnified 9 times . .	28
15. Typical doping profile of the unitrode devices. . . .	29
16. A Thomson-CSF paralleled transistor structure	30
17. A Thomson-CSF Wafer magnified 9 times	31
18. Typical Type A second breakdown	34
19. Ratio of collector-emitter sustaining voltage to the collector-base breakdown voltage <u>vs.</u> emitter current for different base drive conditions	36
20. Typical Type B second breakdown	38
21. Typical Type C second breakdown	39
22. V_{SB} <u>vs.</u> I_{BR} for two collector current densities, J_{CM} $= 18 \text{ A/cm}^2$ and 55 A/cm^2 , in two Unitrode devices. . .	40

23. V_{SB} vs. I_{BR} for two collector current densities, J_{CM} = 64 A/cm² and 82 A/cm², in two Unitrode devices. . . . 41
24. Maximum collector current (at turn-off) vs. second breakdown voltage 42
25. I_{CM} vs. V_{SB} for Type A breakdown. 43
26. I_{CM} vs. V_{SB} for Type B breakdown. 44
27. I_{CM} vs. V_{SB} for Type C breakdown. 45
28. Storage time vs. reverse base current for several values of maximum collector current 46
29. Time to second breakdown vs. maximum collector current for several values of reverse base current. . 47
30. Time to second breakdown vs. energy dissipated at the collector-base junction before second breakdown 48
31. Time to second breakdown vs. reverse base current for collector current density, J_{CM} , = 18 A/cm² in two unitrode devices. 51
32. Time to second breakdown vs. reverse base current for collector current density, J_{CM} , = 64 A/cm² in two Unitrode devices. 52
33. Time to second breakdown vs. reverse base current for current density, J_{CM} , = 82 A/cm² in two Unitrode devices. 53
34. Maximum collector current (at turn-off) vs. second breakdown voltage 54
35. Time to second breakdown vs. maximum collector current (at turn-off) 55
36. V_{SB} vs. I_{BR} for two collector current densities, J_{CM} = 31 A/cm² and 50 A/cm², for one Unitrode and one Thomson-CSF device. 56
37. V_{SB} vs. I_{BR} for two collector current densities, J_{CM} = 75 A/cm² and 85 A/cm², for one Unitrode and one Thomson-CSF device. 57

I. INTRODUCTION

Transistors are susceptible to a destructive mode of operation known as reverse bias second breakdown (RBSB); this generally occurs when the transistor is switching an inductive load. RBSB appears as a high to low collector-emitter voltage, and low to high collector current, transition. If the collector current is not limited by external circuitry, internal heating caused by high current densities will cause device degradation or failure. Triple diffused or double diffused epitaxial power switching transistors are especially susceptible to RBSB. In power conditioning circuits, it is desirable to turn off the transistor as quickly as possible, requiring a reverse base current drive that will rapidly extract stored charge. The reverse base drive increases the susceptibility of the transistor to RBSB because the reverse base current will affect internal charge dynamics during turn-off.

RBSB was first observed by Thornton and Simmons in 1958 (Ref. 1). They suggested that the reverse base current produces a potential gradient along the emitter-base junction, resulting in a concentration or pinch-in of the current injected from the emitter; this effect, at high currents, could result in a regenerative condition and cause RBSB. The exact nature of the regenerative condition was not discussed. Since the first report by Thornton and Simmons, many theories of RBSB have been proposed. Ford (Ref. 2) proposed a theory in which RBSB occurred when some portion of the collector-base junction reached the intrinsic temperature of the higher resistivity side of the junction. The junction would then be shorted by a conducting region, causing a precipitous drop in voltage. Such a theory implies that a critical amount of energy must be dissipated by the transistor during a certain time period. The relationship between dissipated energy and the time at which second breakdown occurs should be independent of base drive conditions. Morrison and Billette (Ref. 3) proposed that second breakdown occurs by way of nonuniformities in the collector-base junction. A region in the collector with a lower than average breakdown voltage can cause the majority of the emitter current to be concentrated in a small area. This theory requires that the collector-base junction is in avalanche breakdown prior to RBSB. Beatty, Krishna and Adler (Ref. 4) and Hower and Reddi (Ref. 5) have independently proposed that RBSB is triggered by avalanche injection of holes from the collector-epitaxial substrate ($n-n^+$) junction into the base region, turning on the emitter region. The emitter electron current will increase, resulting in an increased injection of holes into the base. Positive feedback develops, resulting in RBSB. This theory requires that the charge density in the collector-base depletion region is mainly determined by free carriers and not by the fixed charges, so that the peak electric field is present at the $n-n^+$ junction, and not at the collector-base junction.

Because of the destructive nature of RBSB, early measurements of RBSB were difficult to interpret because of inconsistent data. When a device was driven into RBSB, it was either destroyed, or the device characteristics were so degraded that reproducible measurements could not be obtained. However, a nondestructive measurement has recently been developed (Ref. 6) which permits driving a transistor into RBSB with no apparent degradation. A similar system was constructed and used in this work to stress and measure the RBSB behavior of a single family of switching transistors from one manufacturer, and of generically related devices from another. Section II contains a description of the test system. Section III presents the results of the measurements and discusses their significance. Finally, Section IV describes additional measurements which should be performed for further elaboration of the physical mechanisms of RBSB.

II. TESTER OPERATION

The test system is based on several interdependent subsystems. To simplify its description, general principles of its operation will be provided first, followed by a more detailed discussion of the various subcircuits.

GENERAL DESCRIPTION OF THE TESTER

A simplified schematic of the test system illustrating the arrangement of its components is shown in Figure 1. A forward current pulse, which turns on the device, is applied to the base of the test transistor (TUT). The initial state of the TUT may be controlled by setting the collector supply voltage and the forward base drive pulse width and amplitude. After the forward pulse has been on long enough to drive the transistor into its desired state, a reverse current pulse is applied to the base, and the device begins to turn off. At the end of the storage time, the collector emitter voltage (V_{CER}) increases rapidly to several hundred volts because of the energy stored in the load inductor. Second breakdown is exhibited as a high to low voltage, low to high current transition. The detection capacitor at the collector node detects the rapid fall in V_{CER} , typically 500 V in 10 to 20 ns, and activates the crowbar circuit, diverting destructive collector current within 100 ns through the -140 V energy dump to ground. When the crowbar circuit fires, the diode in the diode inductance circuit shunting the crowbar and the crowbar supply become forward biased, placing the inductor across the crowbar; this reduces the stray inductance between the TUT load inductance and the crowbar circuit.

DETAILS OF THE TEST SYSTEM

Reverse base drive circuit--A block diagram of the base drive circuit and its support circuits is shown in Figure 2. Circuit operation begins with initialization of a timing circuit. Timing circuit operation depends on the selection of either a manual or a triggered start. If the manual start is selected, all inputs to the NOR logic are initially zeroed, gating on the high voltage clamp and collector supply. After a five second delay which allows stabilization of the collector and clamp supplies, a timing pulse is fed to the monostable multivibrator which generates the forward pulse shape. If the triggered start is selected, there is no five second delay between input pulses, permitting repetitive testing. The forward base pulse width may be varied from 1 μ s to 100 ms in a 1-2-5-10 sequence. This pulse is fed to a variable voltage amplifier which operates as the fine tuning control of the forward base current pulse. Output gain is continuously variable between 1 and 2.5. The output pulse of the voltage

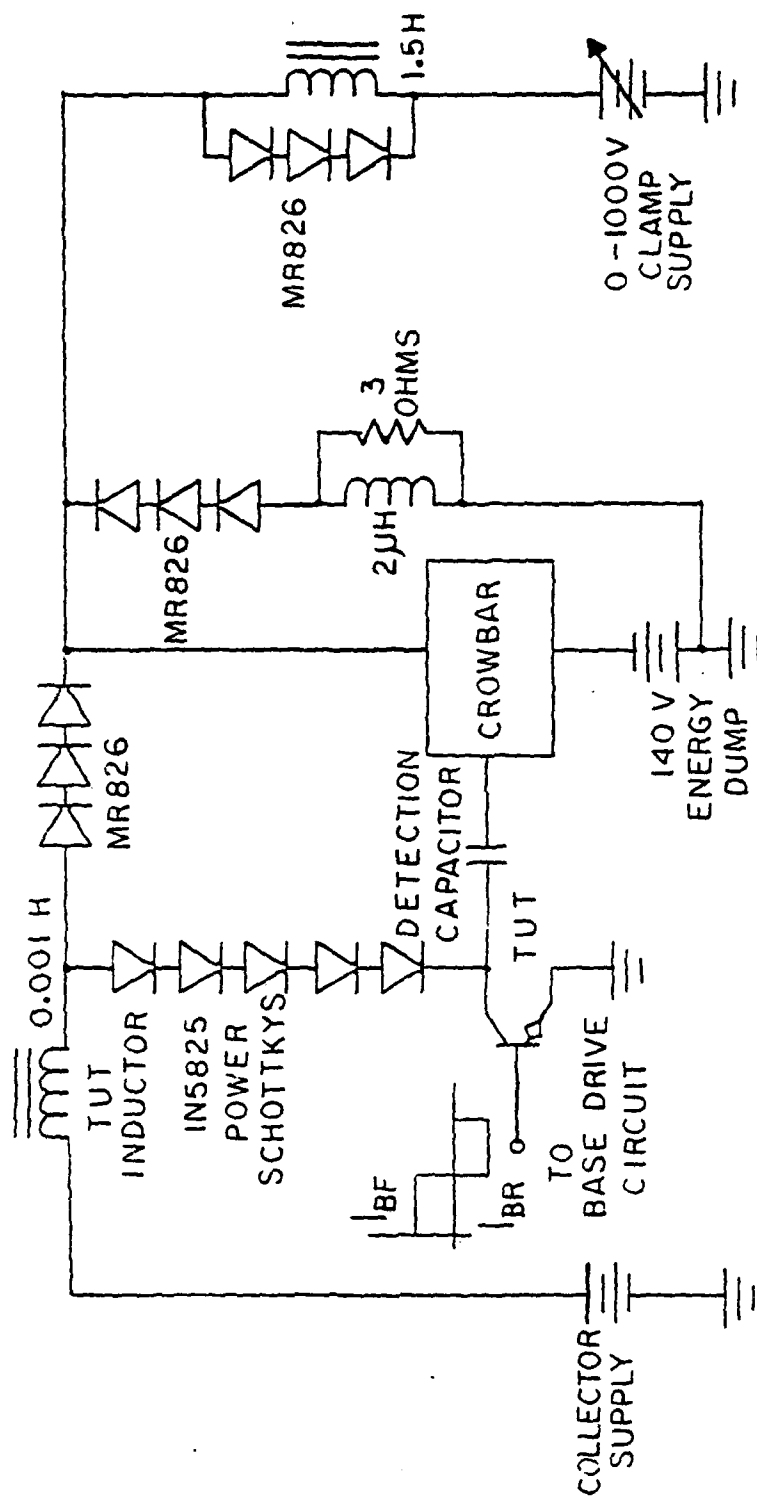


Figure 1. Simplified schematic of the tester.

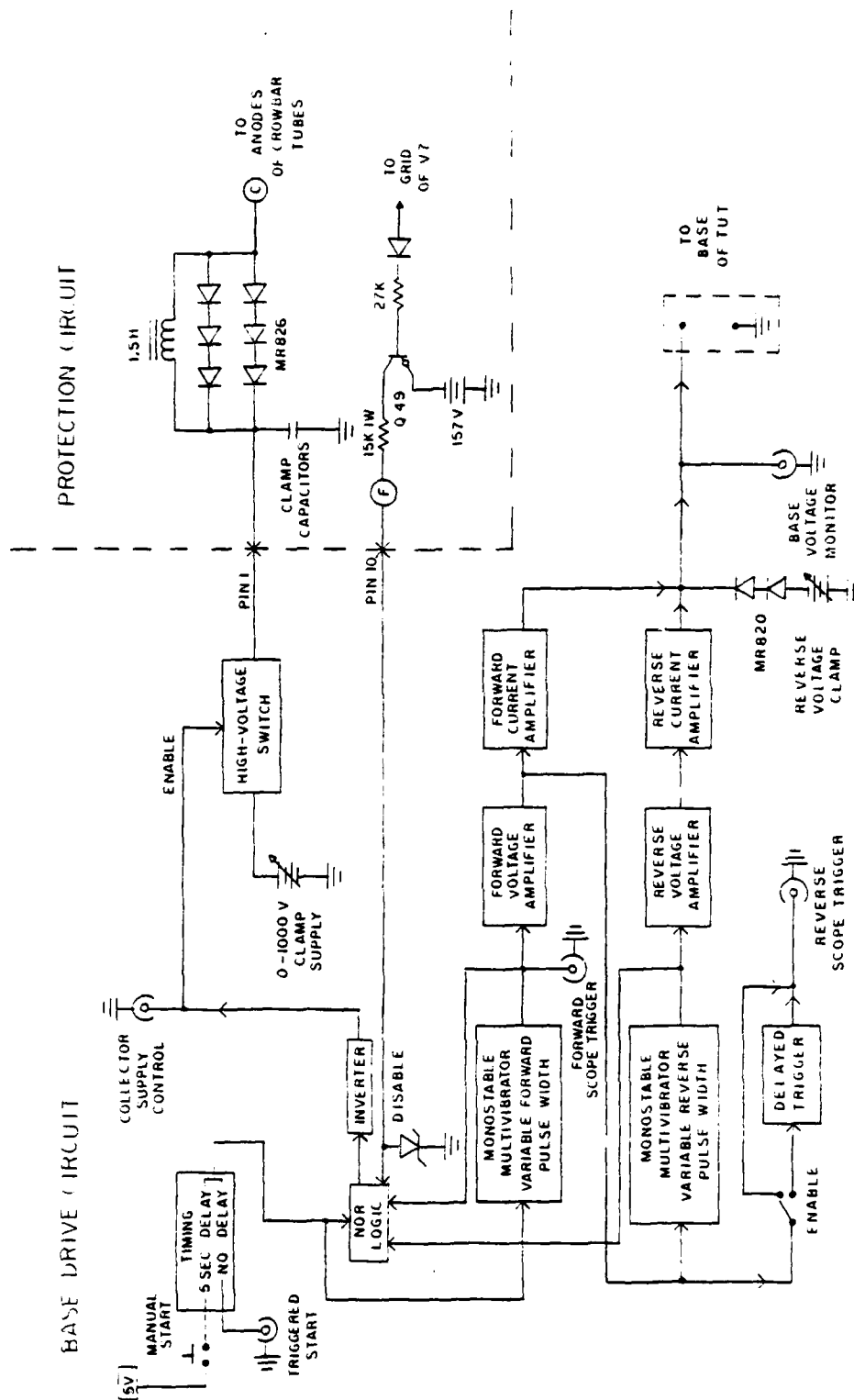


Figure 2. Block diagram of base drive circuit.

amplifier is fed to a variable gain current amplifier which produces the coarse control for the forward pulse amplitude. Coarse settings are 0.01, 0.02, 0.05, 0.1, 0.2, 0.5, 1, 2 and 5 A. The forward base current amplitude is limited to two amperes because the 2N6437 transistor connected in the output stage of the forward current amplifier saturates; further increases in output current then become load dependent.

The reverse base current pulse is initiated by a timing pulse from the forward voltage amplifier. This pulse triggers another monostable multivibrator which is biased for negative logic. The reverse base pulse width may be varied between 1 μ s and 100 ms in a 1-2-5-10 sequence. This pulse is fed to a reverse voltage amplifier which is the fine tuning control of the reverse base current pulse. Output gain is continuously variable from 1 to 2.5. The voltage pulse is applied to a reverse current amplifier which is the coarse control for the reverse base current pulse. Coarse settings are 0.05, 0.1, 0.2, 0.5, 1, 2 and 5 A. The reverse base current amplitude is limited to seven amperes because the 2N6338 transistor connected in the output stage of the reverse current amplifier saturates.

At the end of the forward base pulse, there is a 100 ns delay before the reverse pulse begins, probably because of charge stored in the base of the output transistor in the forward base drive circuit. Another 300 ns elapse before all the transients contained in the reverse base pulse decay, and a constant reverse base pulse is obtained. These transients are probably associated with stray reactances at the base lead. Second breakdown data during the first 100 ms of reverse base drive are therefore not considered significant.

A variable reverse voltage clamp in series with two MR820 diodes is connected to the base of the TUT, so that the emitter-base voltage, V_{EB} , can be limited to a value under the rated TUT base-emitter breakdown voltage. If V_{EB} exceeds the clamp setting during reverse base drive, the constant reverse base current is diverted from the base of the TUT through the clamp supply, limiting V_{EB} to the clamped value. The clamp voltage may be varied from 2 to 13 V. Trigger pulses associated with forward and reverse base drive are fed to the oscilloscope so that the TUT response traces may be captured and displayed. There is no delay introduced relative to the forward base pulse, but the reverse pulse trigger may be delayed continuously between 0.75 and 48 μ s by varying the elements of an RC network. Discrete changes in capacitance provide coarse settings, and continuous changes in variable resistance provide fine settings. Analysis of the delay circuit provides the following expression for the delay time:

$$t_d = M(0.75 + 0.075T) \text{ s} \quad (1)$$

where M is the multiplier (capacitance) setting and T is the number of clockwise turns of the variable resistor.

Collector and high voltage supplies are gated off by the NOR logic in one of two ways, when the crowbar fires, or, if the device does not go into RBSB, when the reverse base pulse turns off. If the TUT does not go into second breakdown, then, after the reverse base drive is off, all inputs to the NOR logic become low and the supplies are turned off. If second breakdown occurs, the six volt zener diode becomes reverse biased, disabling the NOR logic, so that the supplies are turned off even if reverse base drive is still on.

Protection circuit--A block diagram of the protection circuit is in Figure 3. When second breakdown occurs, the collector-emitter voltage usually decreases by about 500 V in 10 to 20 ns. Such a rapid fall in voltage is detected by the detection capacitor at the collector. Physically, this capacitance consists of two small loops of wire, one tied to the collector and the other to the input transistor of the protection circuit; these are separated by some distance determined by the required value of capacitance. The detection capacitance is made small enough so that only high dV/dt rates are detected. The normal fall time of the TUT collector-emitter voltage when second breakdown does not occur is about 500 V in 1 μ s. This value of dV/dt is not detected. The transistor at the input of the protection circuit is in the emitter follower configuration. Its output is fed to two other emitter follower stages, their outputs are fed to four others, and the cascading is continued until sixteen transistors are being driven. The outputs of each of these emitter followers are connected to another transistor circuit which is tied to the control and screen grids of sixteen 6LF6 pentodes. These are tied in parallel to obtain the crowbar. The details of the protection circuit are shown in Figure 4. (This illustration is a duplicate of Figure 12 in Reference 6.) Vacuum tubes are used as the crowbar elements instead of transistors because the slew rate of tubes is higher at higher voltages. The tube anodes are connected in parallel at point C (Fig. 3), and the cathodes are tied together at the -140 V energy dump. The parasitic inductance at the tubes in the crowbar and the parasitic capacitance at the collector of the TUT cause ringing in the collector current when the crowbar fires, so that complete diversion through the crowbar does not occur until ringing is complete, in around 100 ns. This value depends somewhat on the high voltage clamp setting. After the tubes have turned on, a momentary latch timer is triggered and the crowbar circuit is latched on for 0.5s after it initially fires. The crowbar circuit is then reset by the latch timer in preparation for the next test. The momentary latch timer thus limits repeated testing to a maximum frequency of 2 Hz.

When the high voltage clamp supply is gated on, any stray capacitance between the anodes and the cathodes of the sixteen

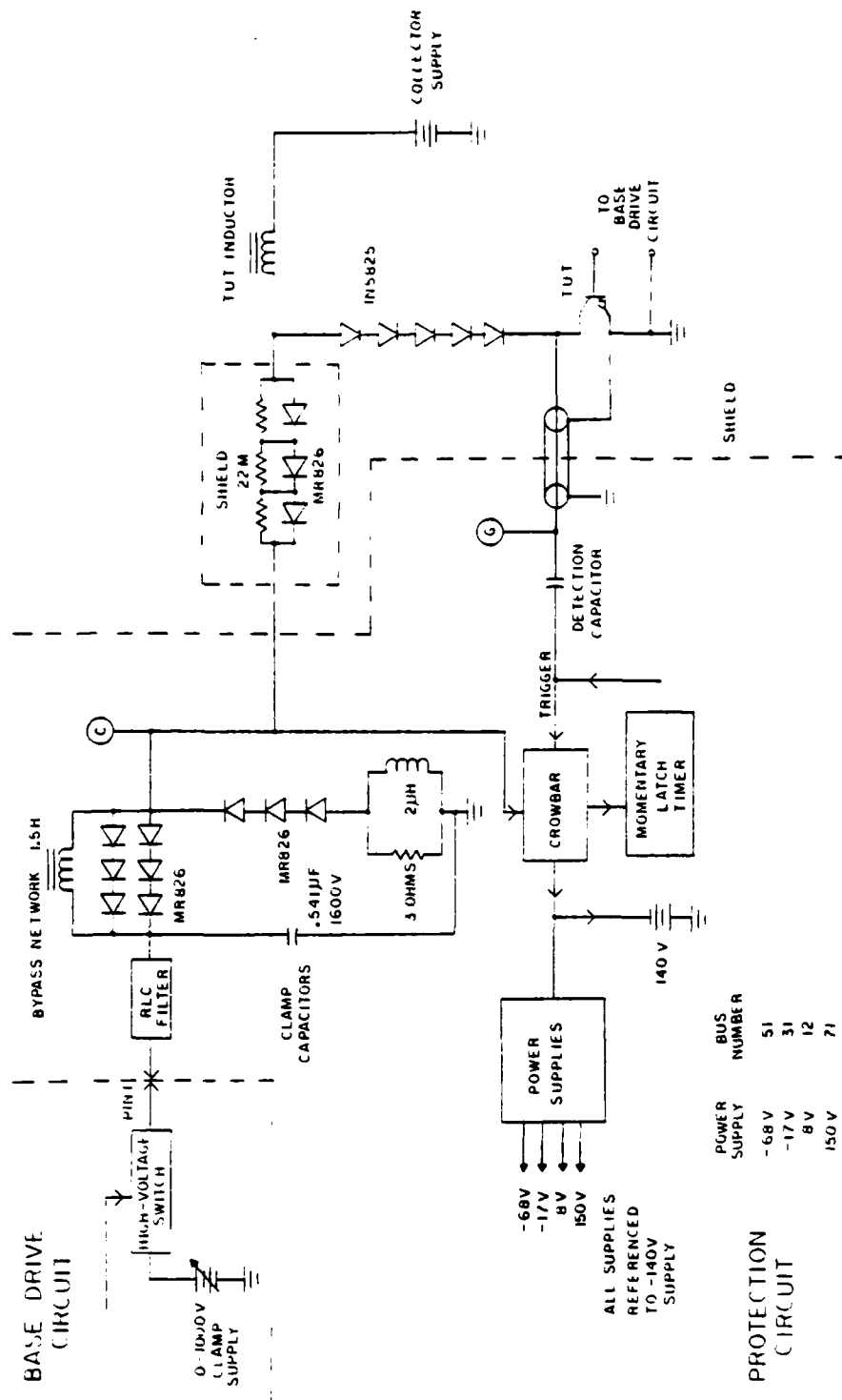
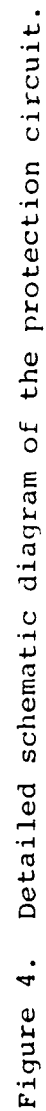


Figure 3. Block diagram of the protection circuit.



pentode tubes are charged to the clamp supply voltage through the 1.5 H inductor. This insures that the collector-emitter voltage is clamped to the full clamp supply during testing. If the collector-emitter voltage exceeds the clamp supply, current flowing in the TUT inductor is diverted to ground through the MR826 diodes and clamp capacitors comprising the bypass network. The collector-emitter voltage remains clamped at this value until all the energy stored in the TUT inductor is dissipated.

Five D.C. power supplies are used in operating the protection circuit. A detailed schematic of the power supplies for the protection circuit is given in Figure 5. The energy dump contains the -140 V high energy supply and two 8300 μ F capacitors, each charged to 70 V which speed up energy dumping. The four other supplies are all referenced to the -140 V supply. A -68 V supply is used for biasing the collectors of the transistors which drive the grids of the tubes (and which are driven by the emitter followers), and for the tube grid bias. A -17 V supply is connected to the collectors of the emitter follower transistors which are used to divide the capacitive input signal. A +8 V supply provides emitter bias for all the transistors. The fourth D.C. supply is a +150 V source for the screens of the tubes. Two 6 V transformers supply the heater current for the tubes. There is a 150 W incandescent lamp connected in series with the primaries of the transformers of the -140 V supply, which limits the current flowing through the supply after second breakdown occurs.

Collector voltage supply--The collector bias source is a low voltage, high current supply with thermal shutdown and current limiting features. The supply is also gated by the timing circuit of the base drive, so that bias may be applied at the time of test, and not before. This feature protects the operator during testing. The supply output voltage is continuously variable to 25 V with a maximum continuous output current of 30 A. A schematic of the supply is shown in Figure 6. Regulation is series pass type and is controlled by a discrete differential amplifier. Thirty power transistors connected in parallel provide the output current.

The thermal shutdown circuit is a discrete differential amplifier with the case of one of the input transistors mounted on the series pass transistor heat sink. If the heat sink temperature becomes excessive, the regulator differential amplifier is disabled, shutting off the voltage supply. The current limiting circuit senses the output current through a 0.15 Ω resistor. If the load current exceeds 3 A for 250 ns, the regulator differential amplifier is disabled. Chassis connections are provided for current limited and unlimited outputs. Current limited outputs are used during the RBSB measurements so that the forward current rating of the IN5825 power Schottky diodes connected in series with the collector of the TUT is not exceeded.

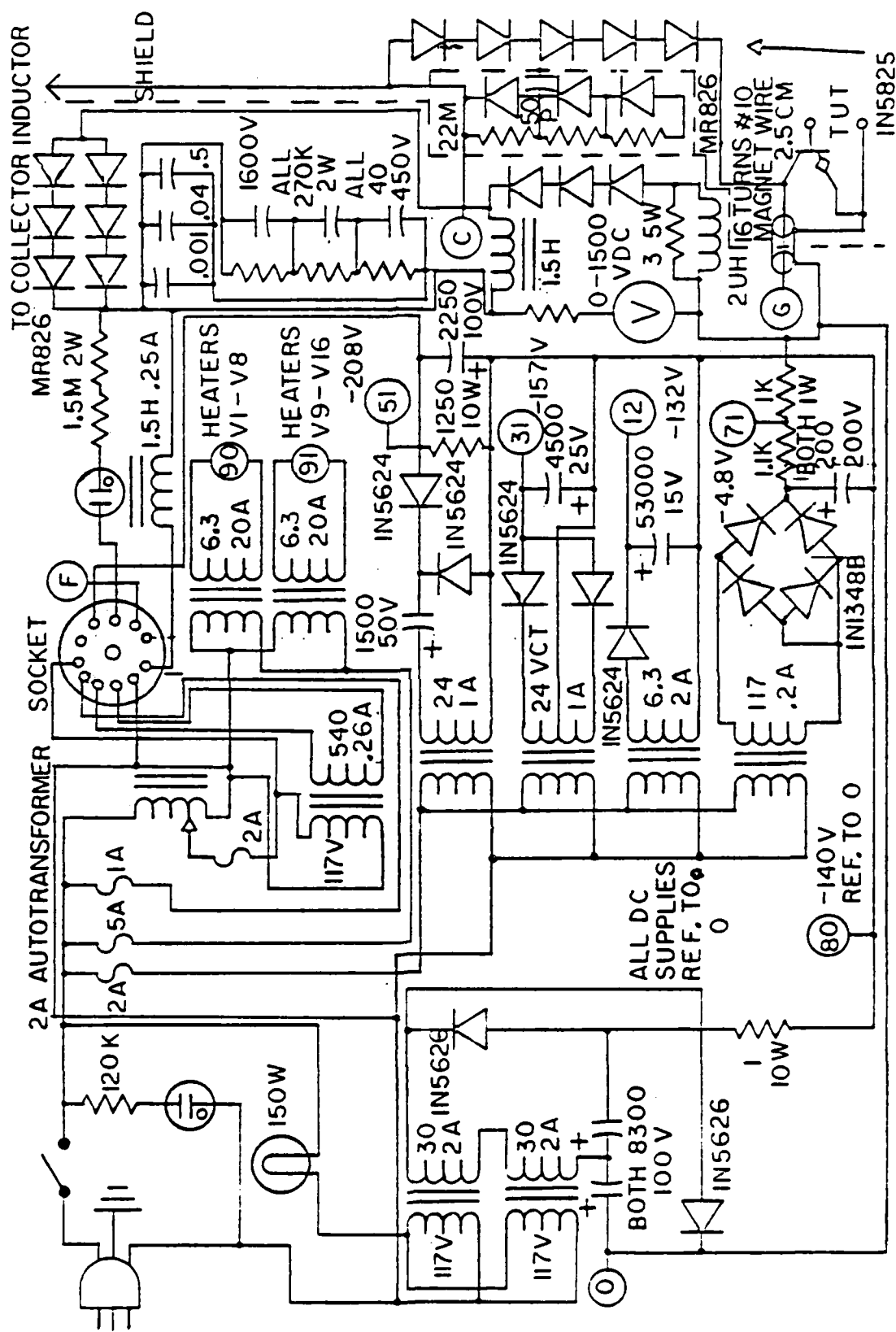


Figure 5. Detailed schematic of protection circuit power supplies.

TUT inductor-- The TUT inductor is a 1 mH inductor constructed from ferrite material which does not saturate at a current of 30 A. This value of inductance provides sufficient energy storage over all ranges of test current. The choke was constructed using 12 Type 3C8 ferrite I cores (bar shaped), 10 cm by 2.5 cm by 2.5 cm. The cores formed a rectangle (a three-core stack per side); a coil consisting of 26 turns of number 10 magnet wire was wound on one side of the rectangle, which was first wrapped with insulating tape. Nonmagnetic restraining blocks were mounted around the core material to secure the inductor. Two small series air gaps, used to fine adjust the value of the inductance, were formed by introducing small pieces of paper into the rectangles at the end of bars.

TUT fixture--The fixture for the TUT was designed for minimal stray capacitance at the collector node. Two transistor sockets, a T0-3 and a T0-15 case type, were mounted in parallel on a rectangular ground plane 5.5 cm by 4.5 cm. The ground plane was tied at each corner and at the center to chassis ground, and was mounted as close as possible to the crowbar circuit to minimize stray inductance. The TUT was mounted in the T0-3 socket; the T0-15 socket was used for connecting the voltage probe to the collector. The stray capacitance of the fixture at the collector node was measured with a Boonton Model 72B capacitance meter to be around 9 pF. The total stray capacitance at the collector node, which was measured to be 80 pF, consists of strays at the collector supply (20 pF), the crowbar circuit (40 pF), and the BNC connections between the collector node and detection capacitor (11 pF). Any stray capacitance at the collector will divert collector current during the time V_{CER} is increasing; this diversion appears as a dip in the collector current at the rapidly rising portion of V_{CER} .

CONSTRUCTION OF THE TESTER

All tester subcircuits, except for the collector power supply, are contained in an aluminum chassis which is subdivided into two sections, front and back. A photograph of the front part of the chassis is shown in Figure 7. Front chassis dimensions are 50.8 x 22.5 x 28 cm. All base drive circuits are housed inside the front chassis with all base drive control setting switches mounted on the outside of the chassis. BNC connections are also mounted on the front chassis for supplying forward and reverse oscilloscope external triggering, for providing the gating control signal for the collector supply, for monitoring the base-emitter voltage, and for supplying an input trigger for repetitive testing. A detailed schematic of the base drive circuit is shown in Figure 8. Figure 9 is a schematic of the voltage regulator circuits for the base drive system. The base drive circuit was subdivided into six subcircuits, each on a separate printed circuit board. The high voltage circuit board contains a D.C. to D.C. gated converter

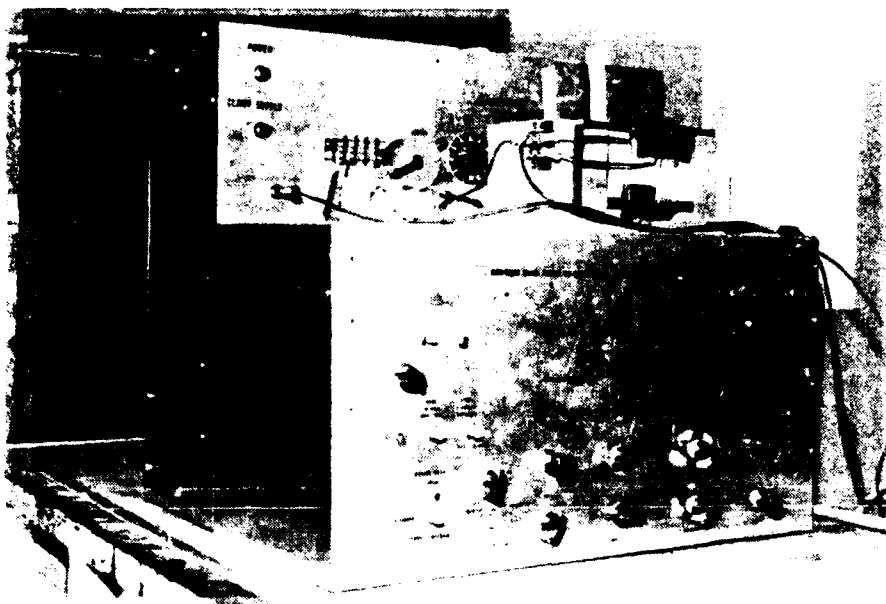


Figure 7. Front chassis of the tester.

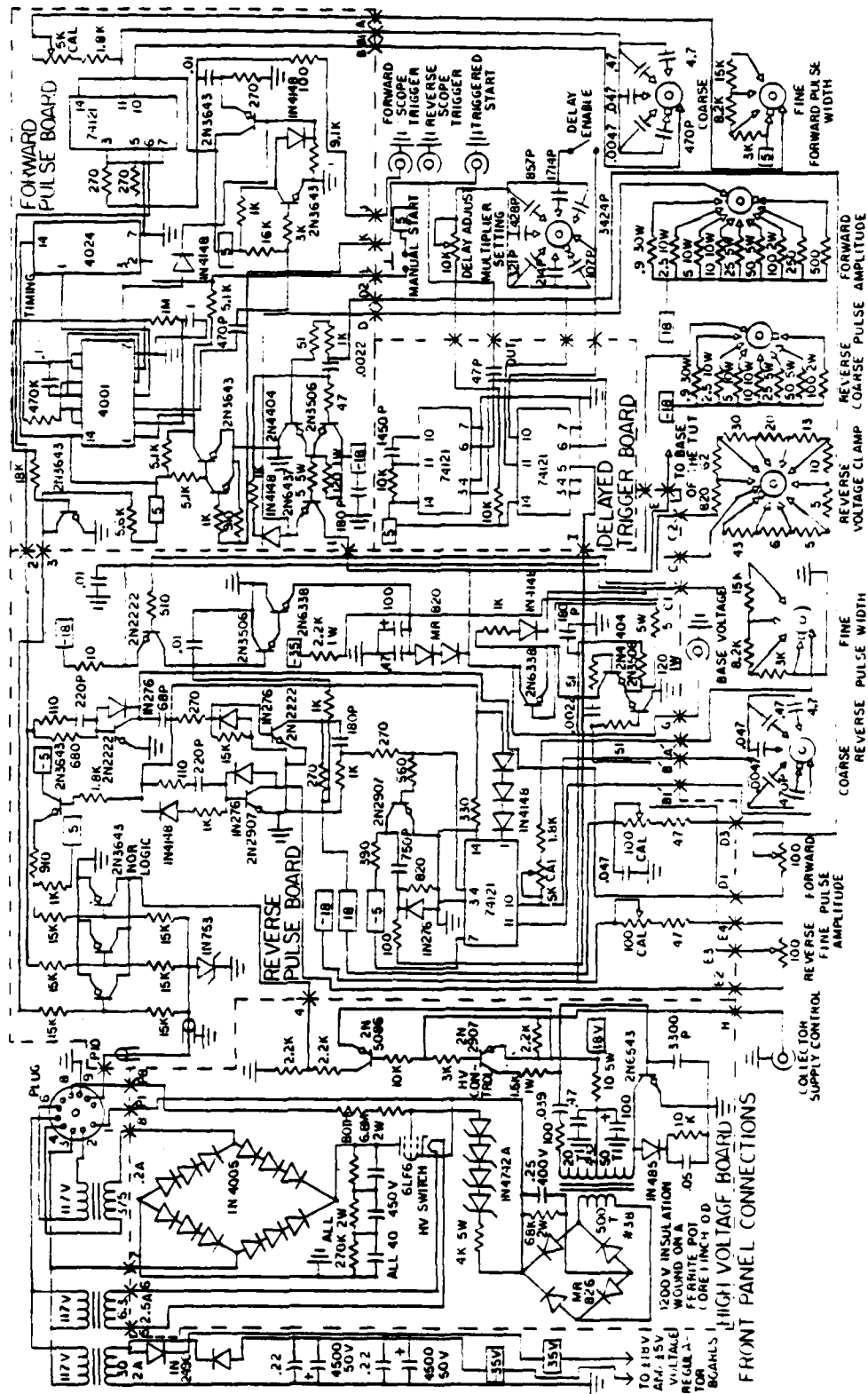


Figure 8. Detailed schematic diagram of the base drive circuit.

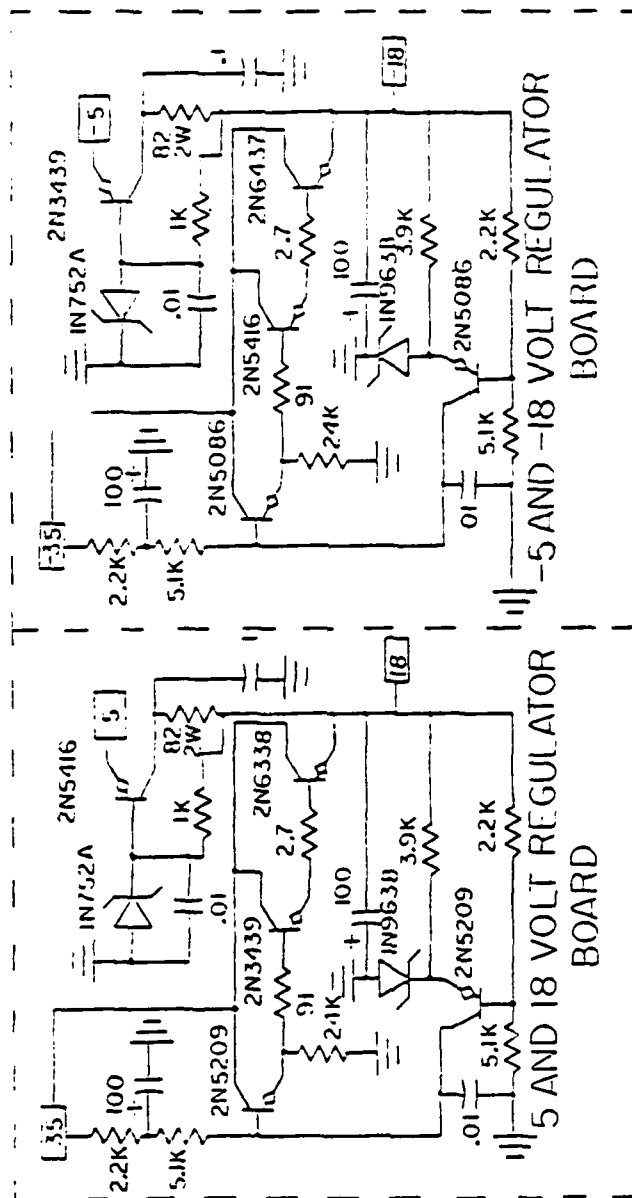


Figure 9. Voltage regulator circuits for the base drive power supplies.

and a high voltage 6LF6 tube used to switch the high voltage clamp supply. The reverse pulse circuit board contains all circuits for the reverse base current drive, and the NOR control logic. The delayed trigger circuit board contains the circuit for delaying the reverse trigger to the oscilloscope. All circuits for the forward base current drive are located on the forward pulse circuit board, which also contains the timing circuit used with the NOR control logic. All switch and BNC connections are shown at the bottom of the circuit schematic. Interconnection points between circuit boards and front panel connections are labeled on the appropriate circuit boards to simplify trouble shooting. The D.C. power supply used for the base drive circuits is a + 35 V, 2 A supply. The regulator boards provide ± 18 V and ± 5 V outputs.

A photograph of the back section of the chassis is shown in Figure 10. Back chassis dimensions are 50.8 x 45.5 x 18 cm. The power supplies for the protection circuit are shown in the lower portion of the picture. The two 8300 μ F capacitors, and the 150 w lamp connected in the -140 V supply is shown at the left center portion of the photograph. The crowbar circuit is at the right center portion of the photograph; it is mounted on a rectangular sheet of aluminum, 35 x 35 cm. The sixteen tubes are mounted on the perimeter of a circle with a 28 cm radius. The symmetry of the crowbar circuit was required because all sixteen tubes must simultaneously conduct when the crowbar is triggered, and the symmetry assures that the strays are the same for each tube. The momentary latch timer is located at the upper right corner on the square sheet of aluminum.

One wire loop of the detection capacitor is connected to the input BNC connector located at the center of the crowbar circuit. The other wire loop is connected to a terminal post to the right of the input BNC connector. The detection capacitance may be increased by decreasing the separation of the wire loops.

The crowbar circuit is mounted to the back chassis with two rectangular support rails. When the top rail is disconnected, the crowbar circuit unfolds, exposing its front portion. A photograph of the front part of the crowbar is shown in Figure 11. The anodes of the sixteen tubes are connected to a terminal post which is isolated from ground. Figure 12 is a photograph of the back chassis with the crowbar circuit folded down. The BNC cable located at the center of the picture is connected to the center BNC connector of the crowbar and is identified as point G in Figure 3. The banana plug at the left of the BNC cable is tied to a terminal post of the anode connections and is identified as point C in Figure 3.

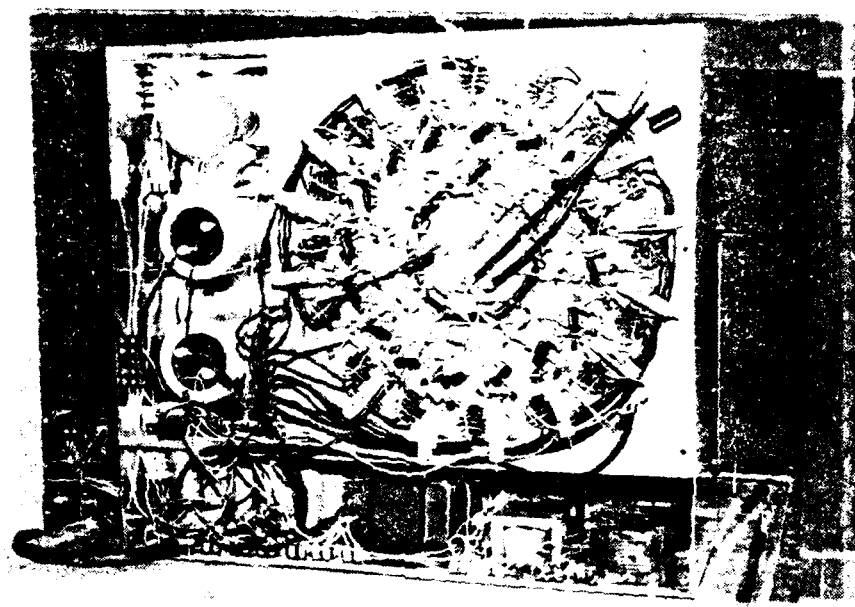


Figure 10. Back chassis of the tester.

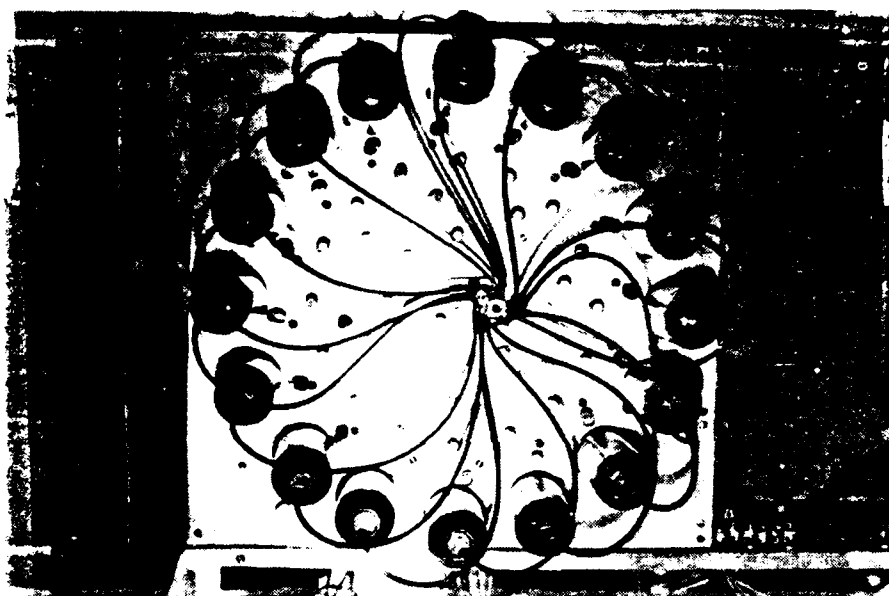


Figure 11. Front part of the crowbar circuit.

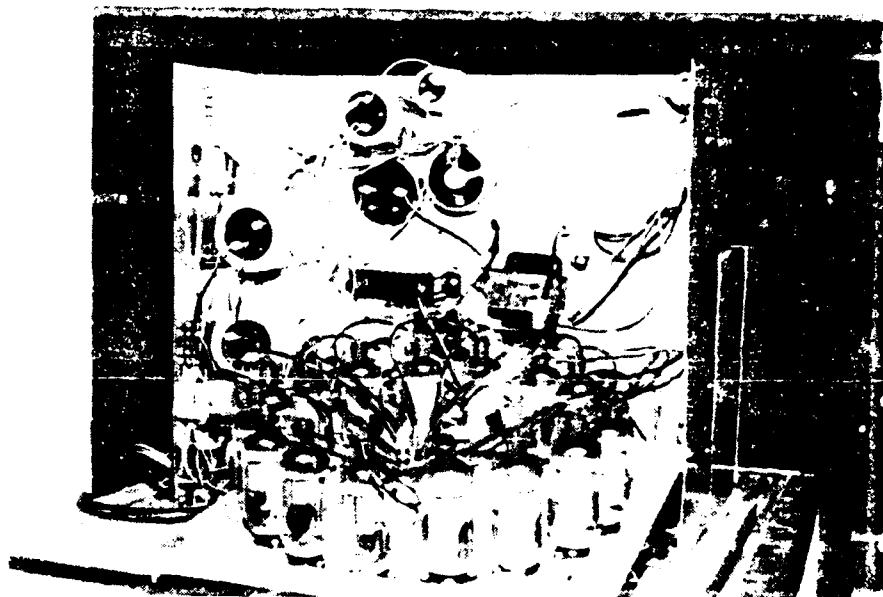


Figure 12. Back chassis with crowbar circuit folded down.

III. EXPERIMENTAL PROCEDURES AND RESULTS

MEASUREMENT SYSTEM

A Tektronix Model 7834 oscilloscope was used to measure second breakdown characteristics. This instrument has a 400 MHz bandwidth. Two Type 7A19 single trace, 600 MHz, 50 Ω input impedance amplifiers were used with a Type 7B80 time base unit to provide a minimum time resolution of around 0.5 ns. The collector-emitter voltage was measured with a Tektronix P6057 100X, 1.4 GHz voltage probe and the base-emitter voltage was measured with a Tektronix P6056 10X, 3.5 GHz voltage probe. The collector current was measured with a Pearson Model 411 current transformer, with a rise time of 10 ns and an output sensitivity of 0.05 V per A.

TEST DEVICES

Two different types of switching transistors were tested. Both types exhibited the same electrical characteristics, but their internal structures were different. For both types, the maximum collector current was 30 A and the sustaining collector-emitter voltage ($V_{CEO(SUS)}$) was 400 V. (V_{CE} has its sustaining value, V_{CEX} , when multiplication at the collector-base junction is large enough to supply sufficient multiplied current to sustain I_F and the reverse base current, I_{BR} . $V_{CEX(SUS)}$ is the minimum value of V_{CEX} . $V_{CEO(SUS)}$ is $V_{CEX(SUS)}$ with the base open, that is, when $I_{BR} = 0$.)

The Unitrode devices were fabricated from two separate masks, in three different lots. (A set of wafers which were processed the same way at the same time is a lot.) The die area for one mask (NH) was 0.22 cm²; the other mask (NE) had a die area of 0.32 cm². One of the lots was fabricated with the NE mask and the other two lots were fabricated with the NH mask. A list of devices contained in each lot is given in Table 1. A photograph of an NE masked structure is shown in Figure 13 and an NH masked device is shown in Figure 14. Each photograph was magnified 9 times. The Unitrode devices are double-diffused, single die structures with an n⁺-epitaxial substrate. A typical doping profile for these structures is given in Figure 15. The base sheet resistance is around 700 Ω/\square under the emitter stripe and about 60 Ω/\square between the emitter fingers. The Thomson-CSF devices are constructed with two triple-diffused dice in parallel, each 0.24 cm² in area. A photograph of the paralleled structure is presented in Figure 16; Figure 17 is a photograph of one wafer magnified 9 times. No lot or doping profile information was provided for these devices.

TABLE 1. IDENTIFICATION OF UNITRODE TRANSISTORS
BY LOT TYPES

Lot Number	Transistor Identification Number
NE-18W	019
	036
	038
220-4	072
	082
	102
	105
220-5	026
	036
	037
	039

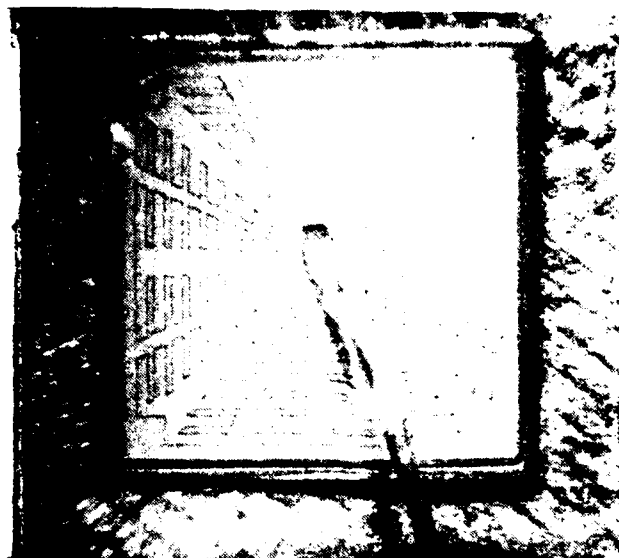


Figure 13. A unitrode NE masked transistor magnified 9 times.

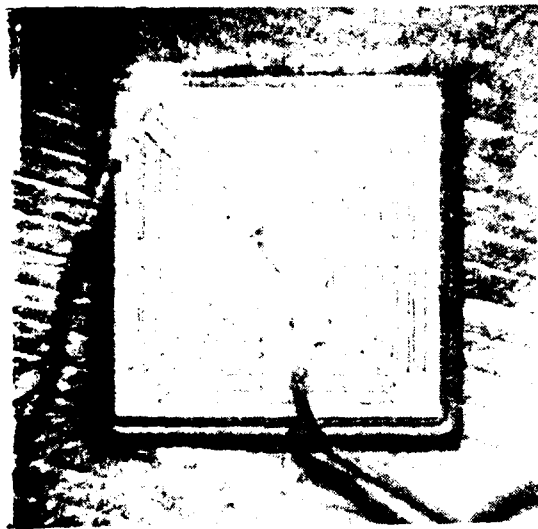


Figure 14. A unitrode MH masked transistor magnified 9 times.

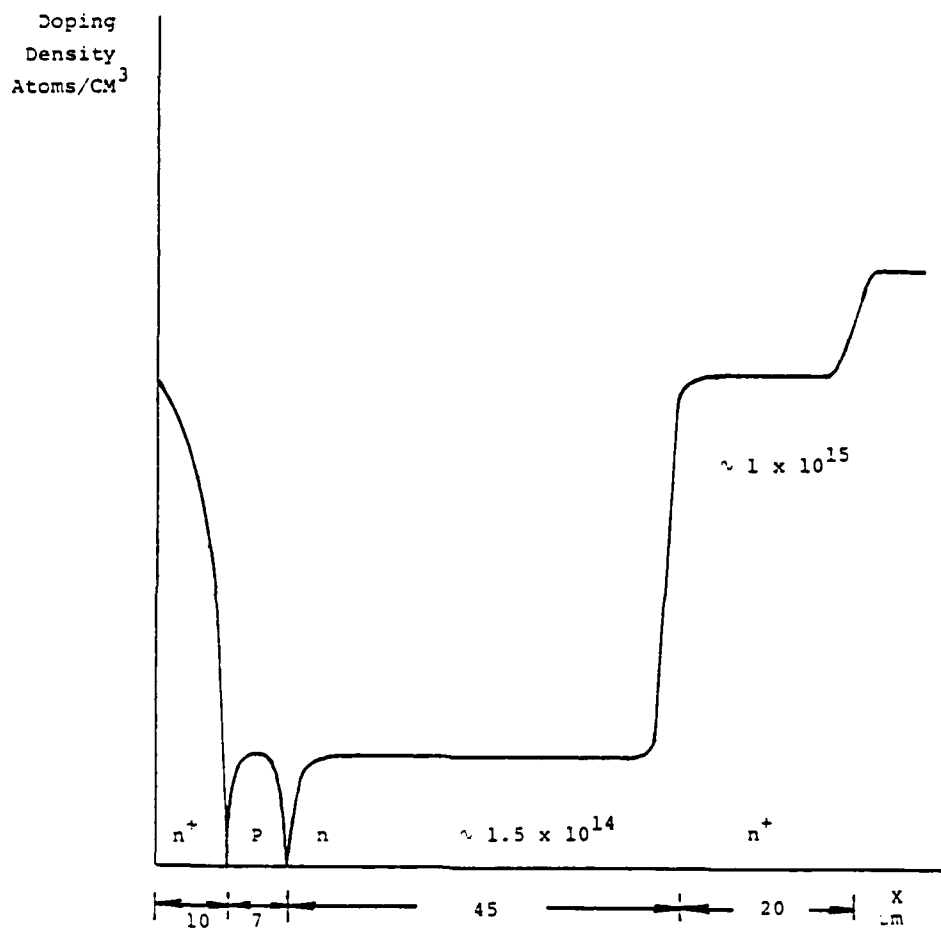


Figure 15. Typical doping profile of the unitrode devices.

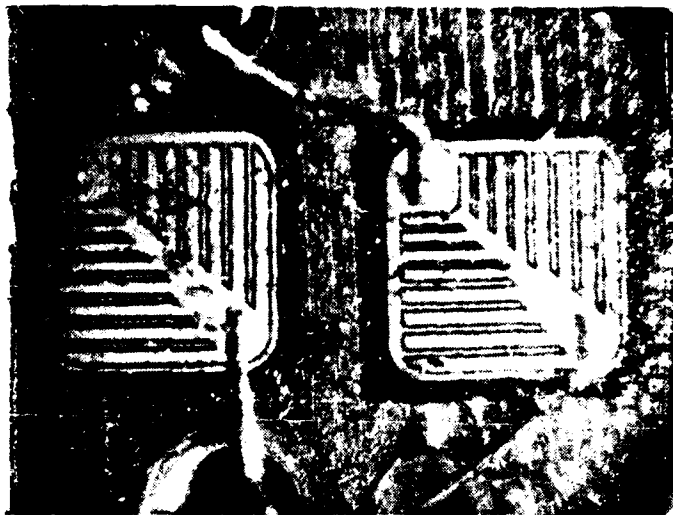


Figure 16. A Thomson-CSF paralleled transistor structure.

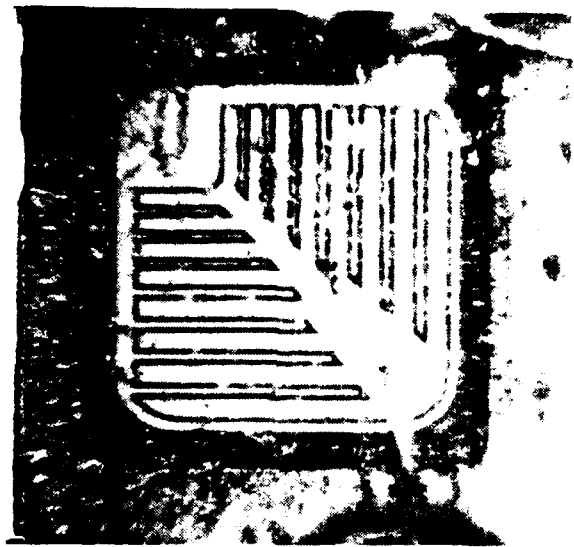


Figure 17. A Thomson-CSF Wafer magnified 9 times.

TEST CONDITIONS

The initial state of the TUT may be controlled by varying the forward current pulse width, t_f , or the collector supply voltage, V_{CC} , or the forward current amplitude, I_{BF} ; only I_{BF} was varied during these experiments. V_{CC} was arbitrarily selected to be constant at 10 V, and t_f was set to 4.5 ms, which is long enough for an adequate base drive but short enough to prevent saturation of the collector current transformer. During testing, the amplitude of the reverse base current pulse, I_{BR} , was held constant while I_{BF} was varied over a wide range of values, typically 15. The values of I_{BR} selected for each device were 0.05, 0.1, 0.2, 0.5, 1, 2 and 5 A. In order to obtain all the data for a single test at one specific value of I_{BF} and I_{BR} , three measurements must be performed, because only a single waveform may be stored on the oscilloscope screen during one horizontal sweep. A typical device was driven into second breakdown 315 times in order to obtain a complete set of data. Inasmuch as 14 devices were tested, 4,410 second breakdown measurements were required to complete the testing. A number of these measurements were repeated and found to be reproducible.

Several parameters were measured during one set of measurements. A list of these parameters is given in Table 2. All time measurements are referenced at the beginning of the reverse base current drive. Photographs of the oscilloscope trace at second breakdown were taken for each device at selected values of I_{BR} and I_{BF} . All time measurements were referred to the beginning of the reverse base current drive.

TYPES OF SECOND BREAKDOWN

It was possible to distinguish three distinct types of second breakdown; these have been designated as Types A, B and C. Typical second breakdown waveforms of the three types are shown in Figures 18, 20 and 21.

Type A (Figure 18)--The initial state of the transistor was either normal active or just in quasisaturation. The TUT reached its sustaining voltage, $V_{CEX(SUS)}$, and remained there for several microseconds before suddenly increasing to the second breakdown voltage. The base-emitter voltage remained positive during sustaining, then rapidly became negative during the time V_{CEX} increased above $V_{CEX(SUS)}$, implying emitter current constriction prior to second breakdown. In the Unitorde devices, the collector current at second breakdown, I_{CSB} , was always much less than the maximum collector current at turn-off, I_{CM} . I_{CSB} was less than or comparable to I_{CM} in the Thomson-CSF devices.

If the collector-emitter voltage reaches $V_{CEX(SUS)}$ before second breakdown occurs, the collector-emitter junction is

TABLE 2. MEASURED DEVICE PARAMETERS

<u>Parameter</u>	<u>Description</u>
V_{CER}	Collector-emitter voltage with reverse base drive
V_{CEX}	Collector-emitter voltage with reverse base drive sustaining conditions
$V_{CEX(SUS)}$	Minimum value of V_{CEX}
V_{SB}	Collector-emitter voltage at second breakdown
V_p	Peak value of the collector-emitter voltage
t_{SB}	Time at occurrence of second breakdown, measured from the beginning of the reverse current pulse
t_s	Storage time (time at which V_{CEX} equals 0.1 $V_{CEX(SUS)}$), measured from the beginning of the reverse current pulse
I_{CSB}	Collector current at second breakdown
I_{CM}	Maximum collector current (at the beginning of turn-off)
V_{BER}	Base-emitter voltage at second breakdown

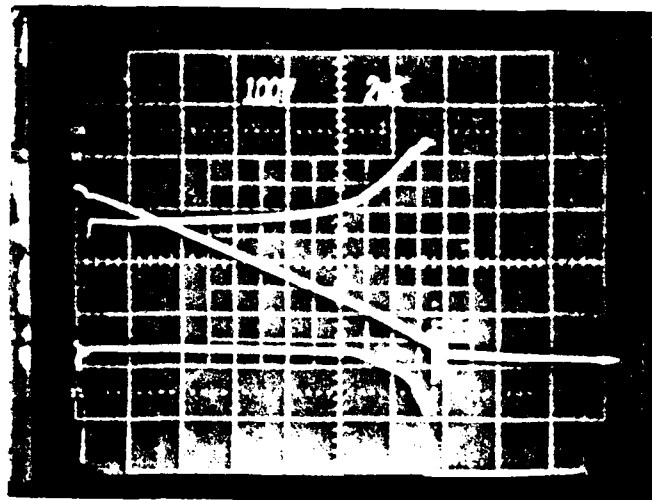


Figure 18. Typical Type A second breakdown. The top curve is V_{CEX} (100V per large division), the middle curve is I_C (2A per large division), and the lowest curve, which decreases to zero and goes negative as V_{CEX} rises, is V_{BER} (2V per large division).

initially in avalanche breakdown. The collector-base multiplication factor, M , must be large enough to supply sufficient charge for recombination in the base, for injection into the emitter, and to maintain a constant base hole current. During turn-off, I_E decreased linearly with time (for all three types of second breakdown). As I_E decreases, M must increase, requiring an increase in V_{CEX} above $V_{CEX(SUS)}$. However, an increase in V_{CEX} is not a sufficient condition by itself for second breakdown to occur. If avalanche breakdown occurs at an isolated region, such as some localized inhomogeneity at the collector-base junction, then an increased V_{CEX} increases the localized carrier generation (Ref. 7); collector current will be diverted to this region, increasing the localized current density. Increased current density increases the net carrier generation rate. The higher density of carriers may exceed the required value for base hole current, base recombination, and emitter injection, so that the emitter is turned on again. A positive feedback mechanism is developed and second breakdown results (Ref. 8). This mechanism alone does not require emitter current constriction, and it is not clear why the emitter current should constrict, unless the inhomogeneity fortuitously lies near the center of the emitter stripe. There may be enough charge stored under the emitter for some Type C behavior to appear. In order to test the validity of this mechanism, Blackburn and Berning (Ref. 9) calculated the ratio V_{CEX}/BV_{CBO} as a function of emitter current and compared their experimental values with values predicted by the dependence of the multiplication factor, M , on V_{CEX}/BV_{CBO} (Ref. 10)

$$M = \frac{1}{1 - \left(\frac{V_{CEX}}{BV_{CBO}}\right)^n} \quad (2)$$

where M is the collector-base multiplication factor; BV_{CBO} is the collector-base breakdown voltage, with the emitter open; and n is a constant which has a value of around 4 for p-type silicon, and the expression (Ref. 11)

$$I_{BR} = (1 - M\alpha) I_E \quad (3)$$

where α is the common base forward current gain. In their calculation, α was assumed to be constant at its maximum value. The value of M required to maintain a constant I_{BR} for a given I_E was substituted in Equation (2) to determine V_{CEX}/BV_{CBO} for that value of I_E ; fair agreement between measured and predicted values was obtained. These calculations were repeated in this work for one Thomson-CSF device at two values of I_{BR} and one Unitrode device at a single value of I_{BR} ; the data are plotted in Figure 19. It was difficult to obtain measurements over a

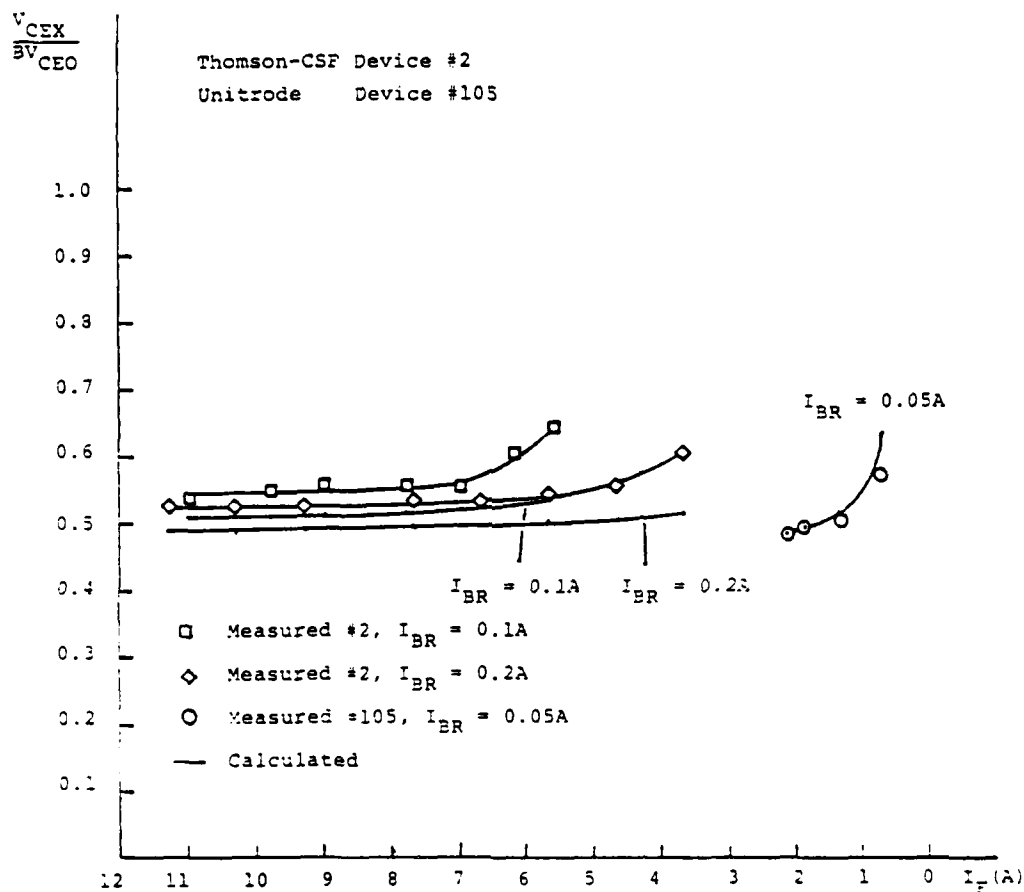


Figure 19. Ratio of collector-emitter sustaining voltage to the collector-base breakdown voltage vs. emitter current for different base drive conditions.

large range of emitter currents because of limited forward base drive (maximum I_E) and the relative high values of I_E at which second breakdown occurred (minimum I_E). The agreement between the calculated and measured values is as good as or better than that obtained by Blackburn and Berning, and suggests that the proposed mechanism is fairly good.

Type B (Figure 20)--The TUT was initially in quasi-saturation. V_{CEX} reached $V_{CEX}(SUS)$ and remained there for a short period of time before second breakdown occurred. The transition between Type A and Type B was quite abrupt. Type B appeared with small increases in I_{CM} , that is, as soon as the device moved into quasi-saturation. The base-emitter voltage was always positive prior to breakdown, implying that the emitter current did not constrict. I_{CSB} was usually comparable to I_{CM} . This type of second breakdown apparently has not been observed before; there is no explanation for it as yet.

Type C (Figure 21)--The initial state of the transistor was quasi-saturation. It did not reach its sustaining voltage before second breakdown occurred. In this case, the base-emitter voltage became negative during turn-off, implying emitter current constriction. This voltage was sometimes negative during the storage time, so that current constriction may begin to occur quite early, during turn-off. I_{CSB} was slightly less than I_{CM} .

When a transistor is in saturation or quasisaturation during turn-on, the base and collector regions are heavily flooded with free carriers, resulting in conductivity modulation. During turn-off, charge is first removed from under the base contacts. Stored free charge is still located under the emitter and provides a low resistance path for current flow. As more charge is extracted, this highly conductive region (the current-induced base) begins to shrink in width, increasing the collector current density, j_C . At high current densities, the peak electric field will shift from the collector-base junction to the n - n^+ collector-epitaxial substrate interface. Avalancheing, followed by hole injection into the base (avalanche injection), occurs at the interface at high electric fields, followed by positive feedback and second breakdown. The concept of a current-induced base is required to explain an increase in collector current density before a sustaining voltage is reached (Ref. 12).

EXPERIMENTAL RESULTS

Unitrode devices--In general, the Unitrode transistors exhibited Type A behavior at low collector currents and reverse base drives; Type B second breakdown occurred for larger collector currents and low to medium values of reverse base current; and Type C breakdown was observed for large collector and reverse base currents. The second breakdown voltages at the three types of breakdown were reasonably close for all devices

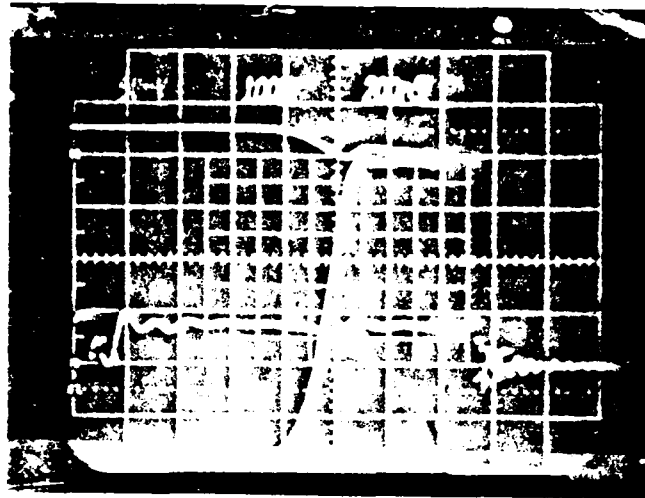


Figure 20. Typical Type B second breakdown. The top curve is I_C (1A per large division), the center curve, which remains positive, is V_{BER} (1V per large division), and the lowest curve is V_{CEX} (100V per large division).

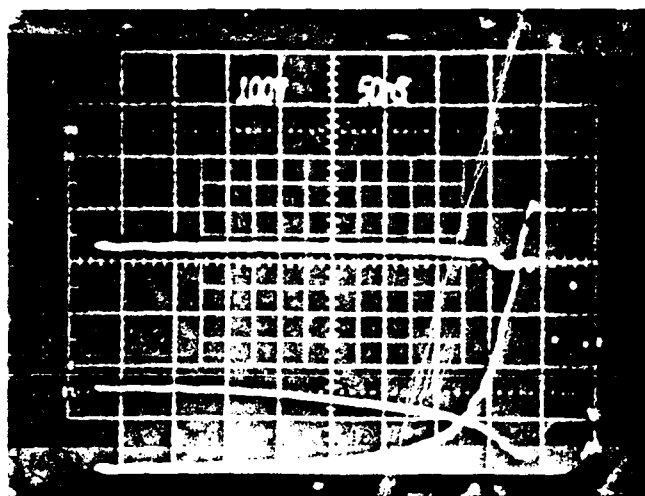


Figure 21. Typical Type C second breakdown. The top curve is I_C (4A per large division), the center curve, which is negative and becomes more negative as the transition turns off and V_{CEX} increases, is V_{BER} (1V per large division), and the lowest curve is V_{CEX} (100V per large division). The oscilloscope trigger was delayed 0.75 μ s relative to the beginning of the reverse base drive pulse in this trace.

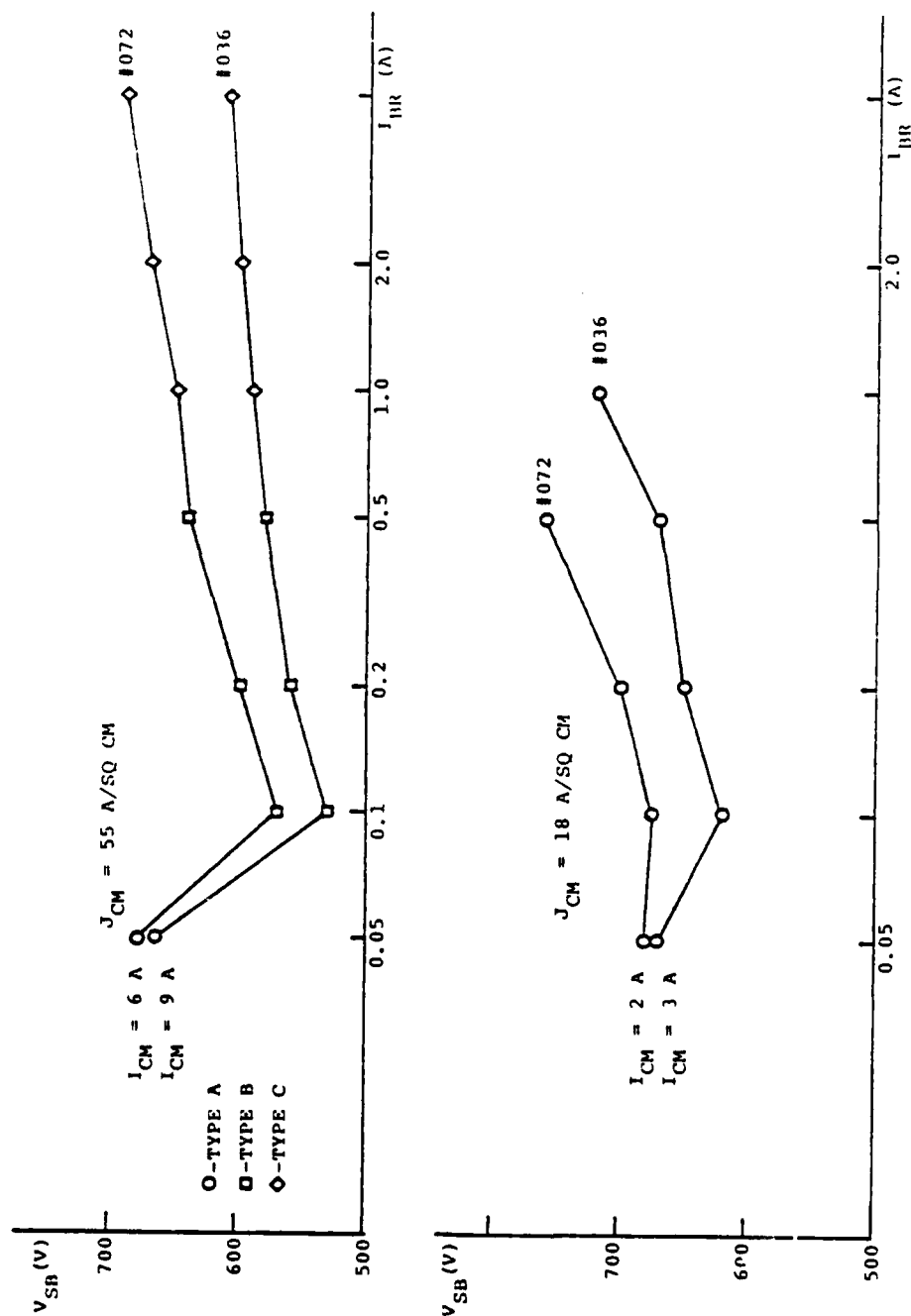


Figure 22. V_{SB} vs. I_{BB} for two collector current densities, $J_{CM} = 18 \text{ A/cm}^2$ and 55 A/cm^2 , in two Unitrode devices.

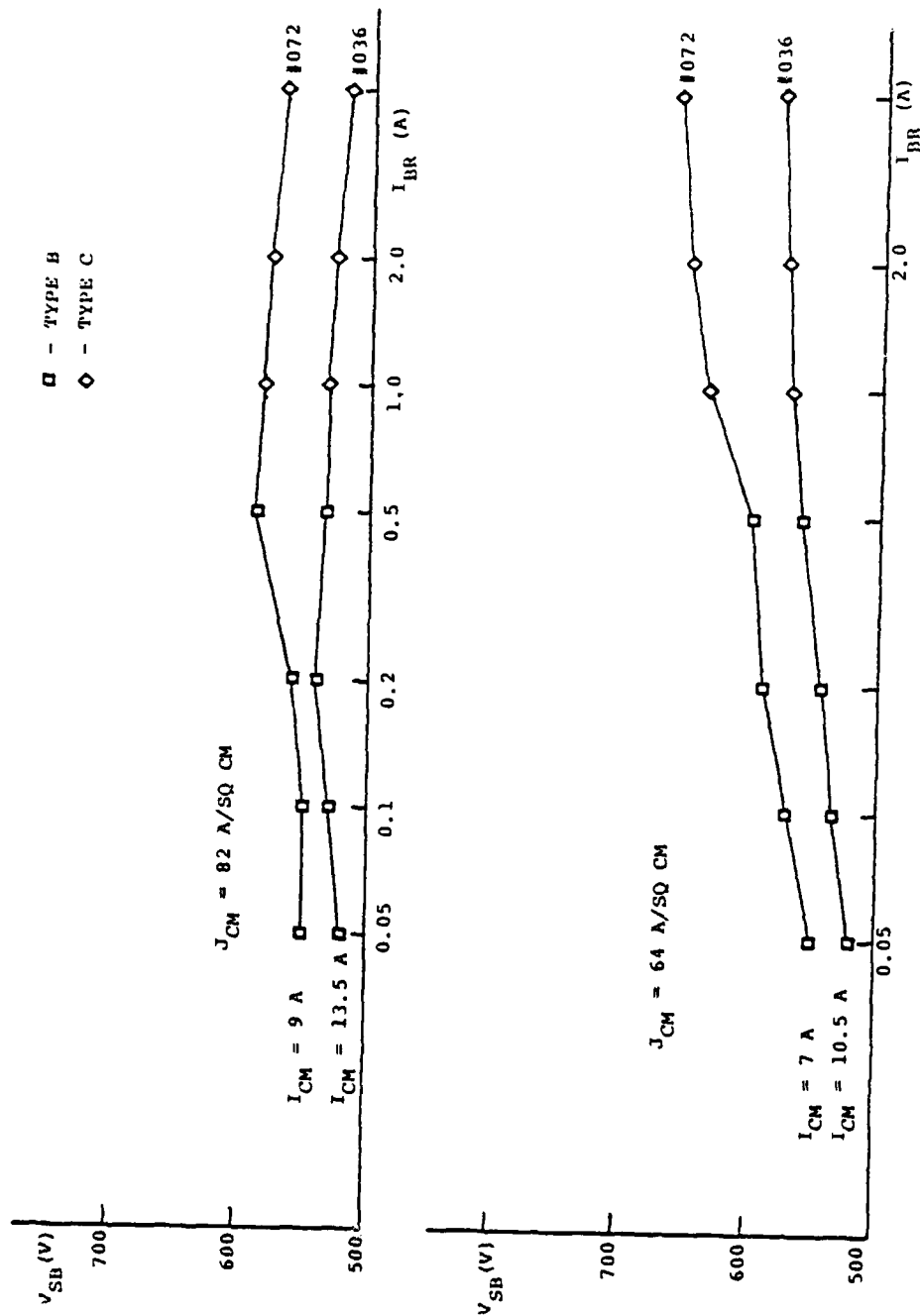


Figure 23. V_{SB} vs. I_{BR} for two collector current densities, $J_{CM} = 64 \text{ A/cm}^2$ and 82 A/cm^2 , in two Unitrode devices.

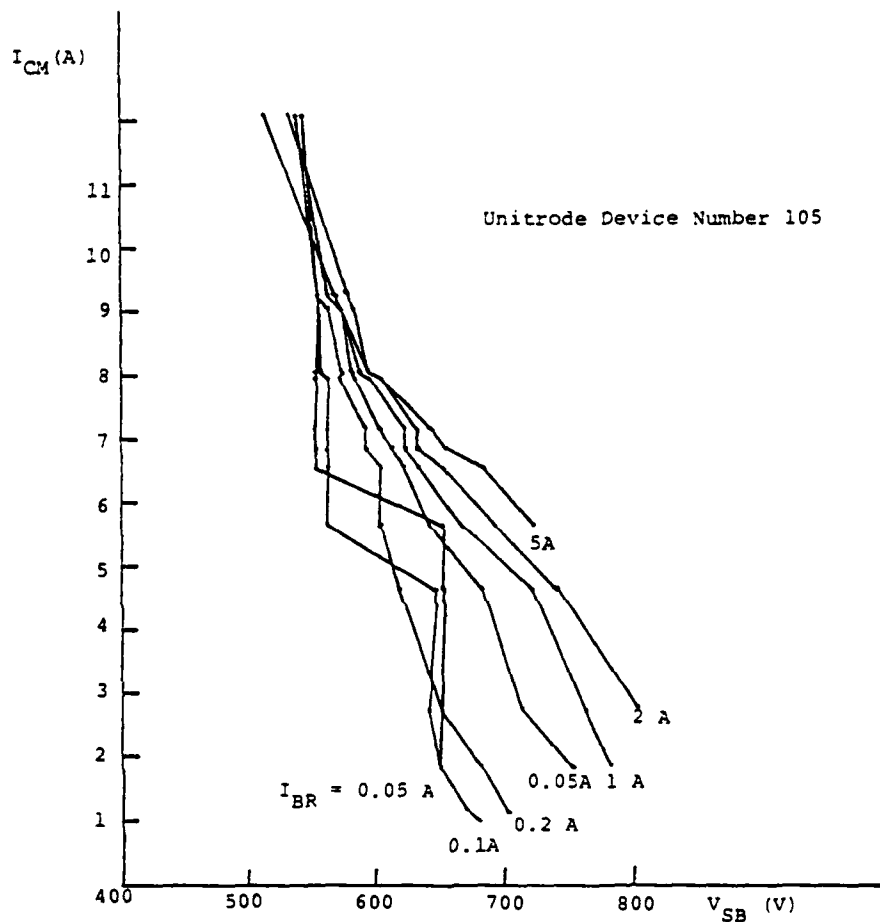


Figure 24. Maximum collector current (at turn-off) vs. second breakdown voltage.

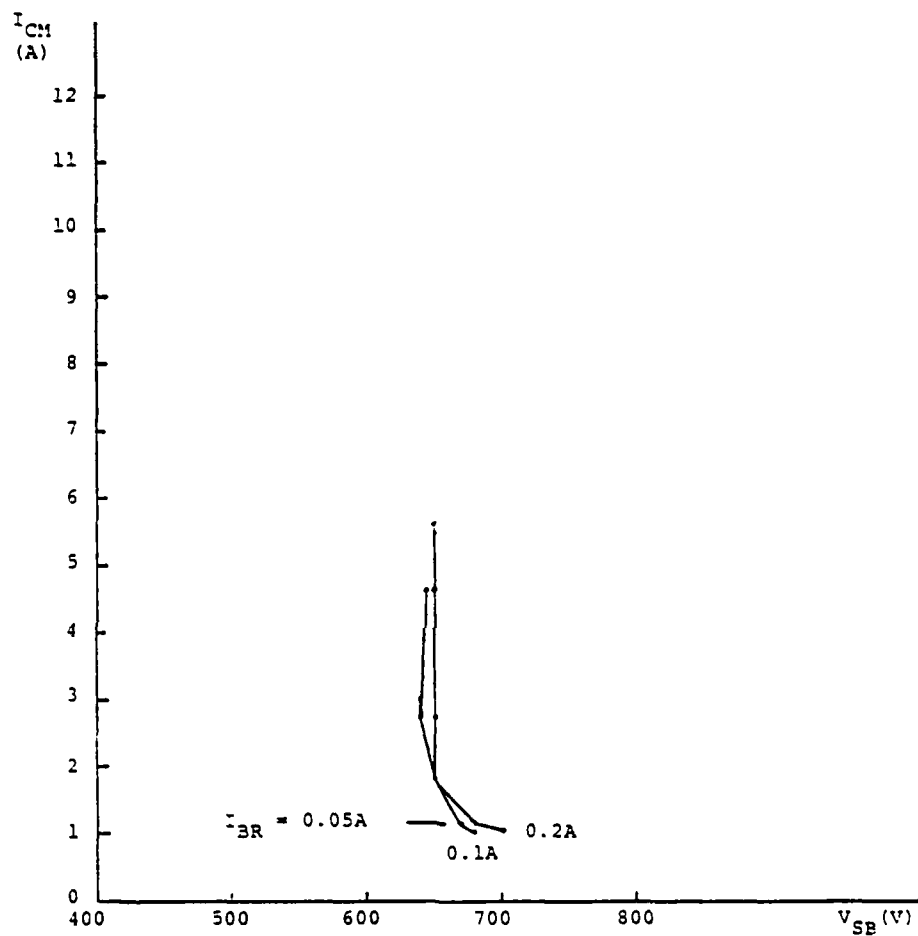


Figure 25. I_{CM} vs. V_{SB} for Type A breakdown.

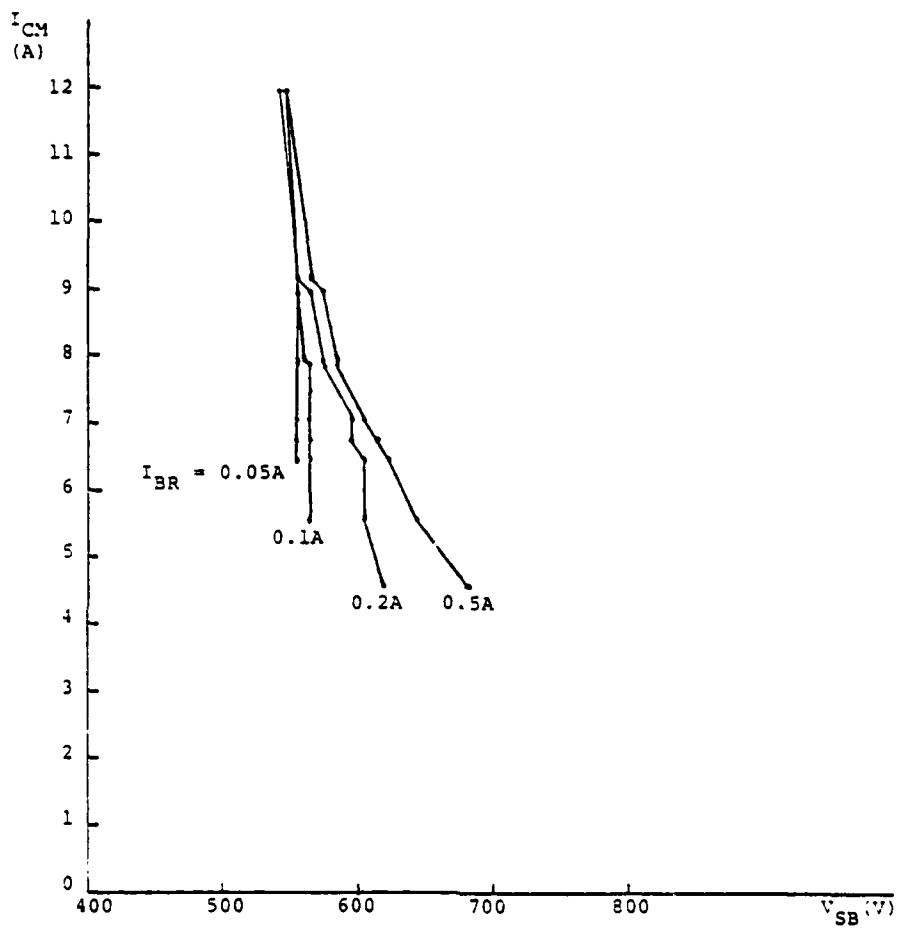


Figure 26. I_{CM} vs. V_{SB} for Type B breakdown.

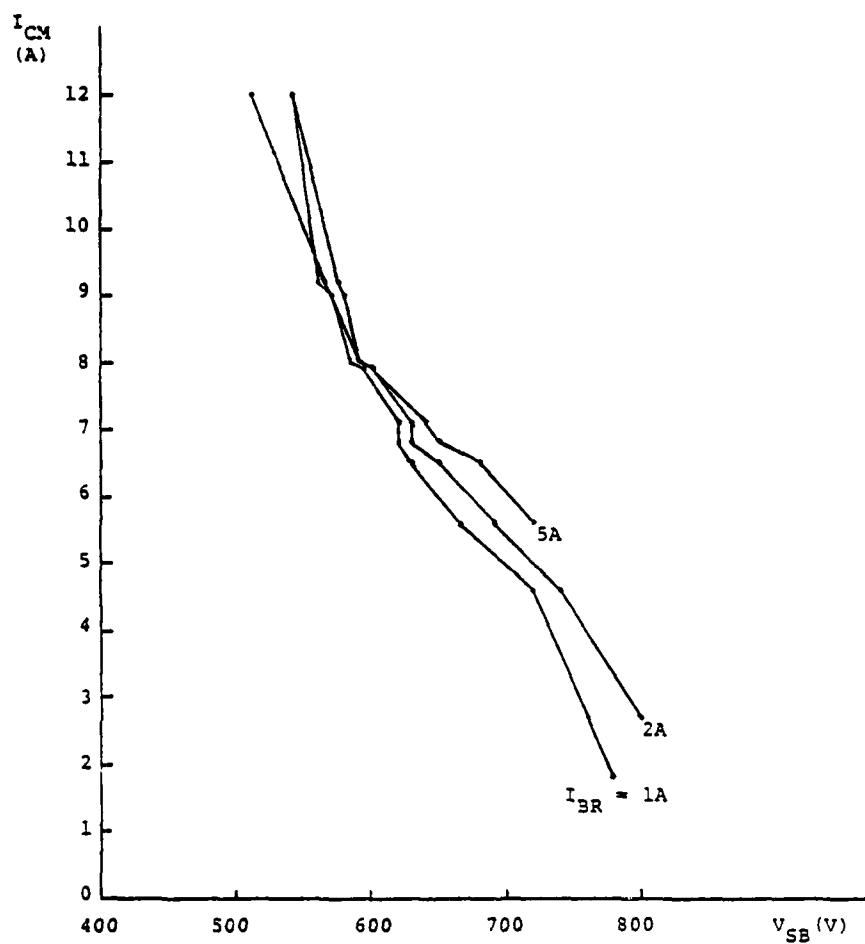


Figure 27. I_{CM} vs. V_{SB} for Type C breakdown.

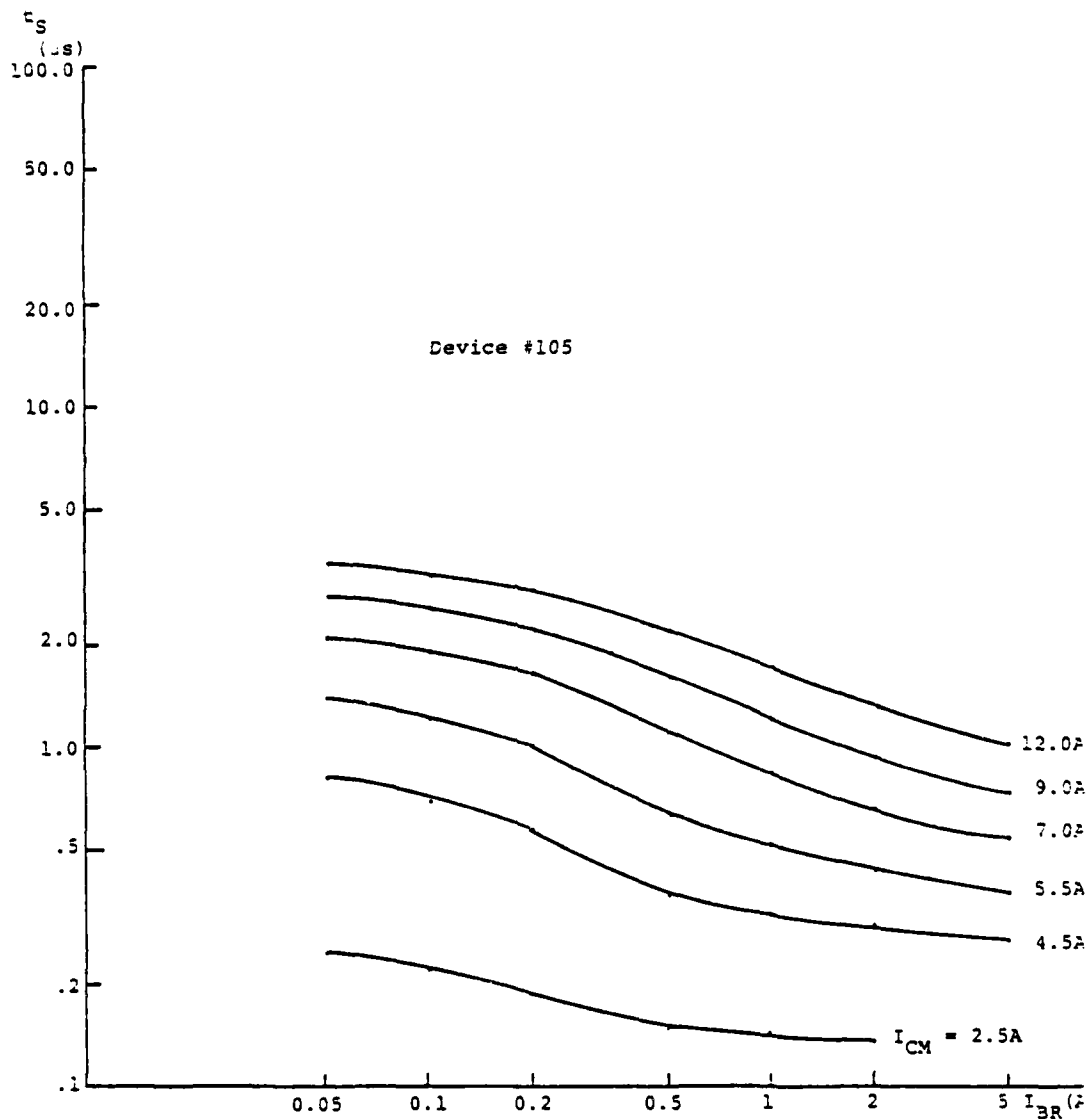


Figure 28. Storage time vs. reverse base current for several values of maximum collector current.

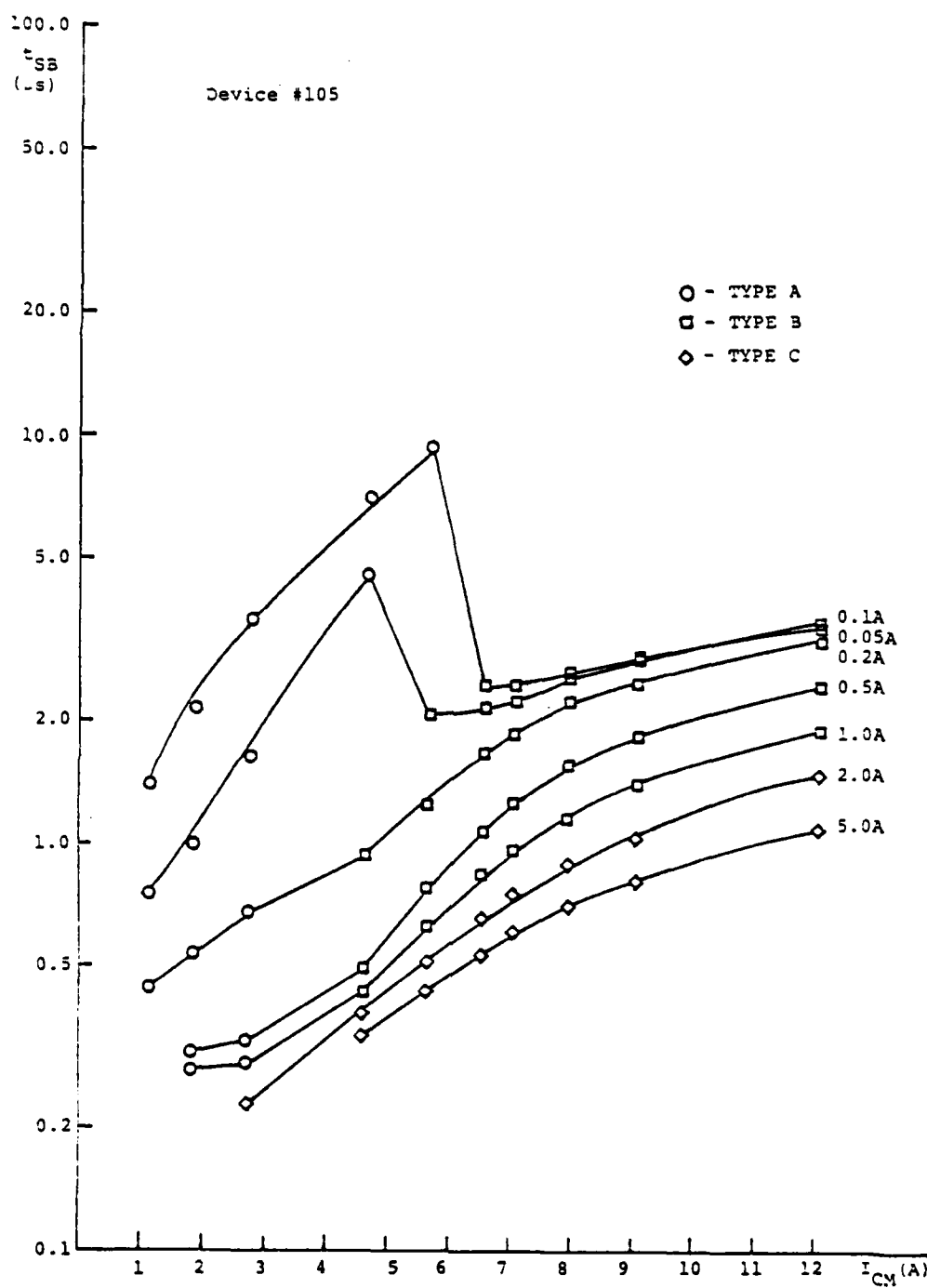


Figure 29. Time to second breakdown vs. maximum collector current for several values of reverse base current.

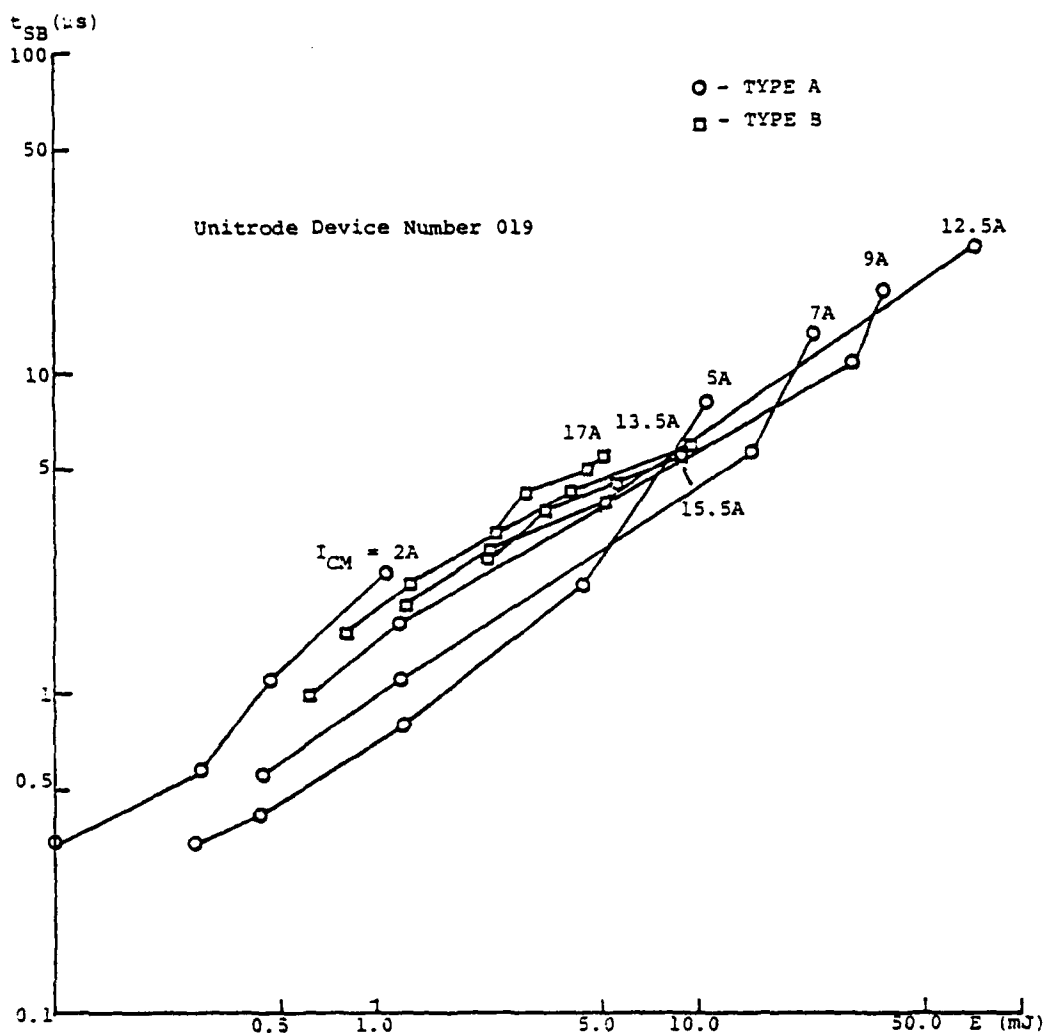


Figure 30. Time to second breakdown vs. energy dissipated at the collector-base junction before second breakdown.

when the collector current was scaled relative to die size, that is, when the comparisons were made as a function of collector current density. (The collector current density was obtained by dividing the total collector current by the emitter area. Although the emitter area can be calculated exactly by measuring the total emitter geometry, it is more convenient to use the approximation that the emitter area is close to one-half the die area (Ref. 13). This approximation was also used in calculating the collector current density in the Thomson-CSF transistors.) Figures 22 and 23 compare second breakdown voltages versus reverse base current for various collector current densities for two devices; the approximate agreement in V_{SB} at a given current density and reverse base drive is typical for all the devices. Figure 24 shows the maximum collector current at turn-off plotted versus the second breakdown voltage for a typical device. These curves are qualitatively representative of the results for all the devices. It is to be noted that, although the curves seem to converge to $V_{SB} = V_{CEX(SUS)}$ for all base drives at high currents, there is actually a trend to lower values of V_{SB} , below $V_{CEX(SUS)}$, at very high collector currents where Type C second breakdown occurs. At low collector currents, V_{SB} increases with increasing base drive. This is probably the result of higher values of the collector-base junction multiplication factor required to sustain the base current and is typical of Types A and B breakdowns, which occur after $V_{CEX(SUS)}$ is reached. Figures 25, 26, and 27 contain the separate data for Type A, Type B, and Type C breakdown, respectively. It can be clearly seen from these that V_{SB} for Type A breakdown converges to $V_{CEX(SUS)}$; that the trend to lower values of V_{SB} begins with Type B, and that no apparent convergence exists for Type C. These data support the argument for different mechanisms for the different types.

As expected, the storage time, t_s , decreases with increasing I_{BR} ; the measured dependence of t_s on I_{BR} and I_{CM} is plotted in Figure 28. The time at the occurrence of second breakdown, t_{SB} , measured from the beginning of the reverse current pulse, always decreased for increasing I_{BR} for all types of second breakdown; however, t_{SB} was much greater for Type A than for Types B and C. Figure 29 illustrates the behavior of t_{SB} as a function of I_{CM} and I_{BR} . It is interesting to examine t_{SB} as a function of the total energy dissipated at the collector-base junction between the time that reverse base current begins to flow and the time that second breakdown occurs; these data are plotted in Figure 30. (The energy calculation is tedious and time consuming, and was performed only for a single device; however, the results are considered representative for all the devices because of the close similarity in behavior between all the devices for the three types of second breakdown.) However, the agreement in t_{SB} at a given I_{BR} for different I_{CM} between devices from different lots is not as good for Type A breakdown as for Types B and C. Figures 31, 32, and 33 compare t_{SB} for the two lots. Type A breakdown may be more sensitive to processing conditions.

Thomson-CSF devices--Only three Thomson-CSF devices were available for study in this portion of the work. Type A breakdown was similar to that in the Unitrode devices; the values of V_{SB} were comparable, but Type A breakdown persisted to much higher values of I_{BR} (up to 5 A) than in the Unitrode devices. Type B breakdown occurred at higher values of I_{CM} and I_{BR} than for the Unitrode devices, although values of V_{SB} for Type B were similar to those in the Unitrode devices. Type C second breakdown was not observed, possibly because the device could not be driven very far into quasi-saturation (forward base drive was insufficient). Figure 34 shows the typical dependence of I_{CM} versus V_{SB} for the Thomson devices. The time to second breakdown, t_{SB} always decreased with increasing I_{BR} , similar to the Unitrode devices. Figure 35 illustrates the dependence of t_{SB} on I_{CM} and I_{BR} .

It is possible to compare the behavior of the Unitrode and the Thomson devices if the collector current densities are considered. Figures 36 and 37 compare the behavior of the second breakdown voltage as a function of reverse base drive for a Unitrode and Thomson device at four values of maximum collector current density. Although the variation in V_{SB} with I_{BR} is similar for the two devices at low collector current densities, their qualitative behavior begins to differ at higher current densities. It is possible that the triple diffused structure behaves differently than the epitaxial structure of the Unitrode device, but this is a very speculative suggestion. A closer comparison of the device structures can not be made at this time because values of base width, and of base and collector impurity densities, have not yet been received from Thomson-CSF.

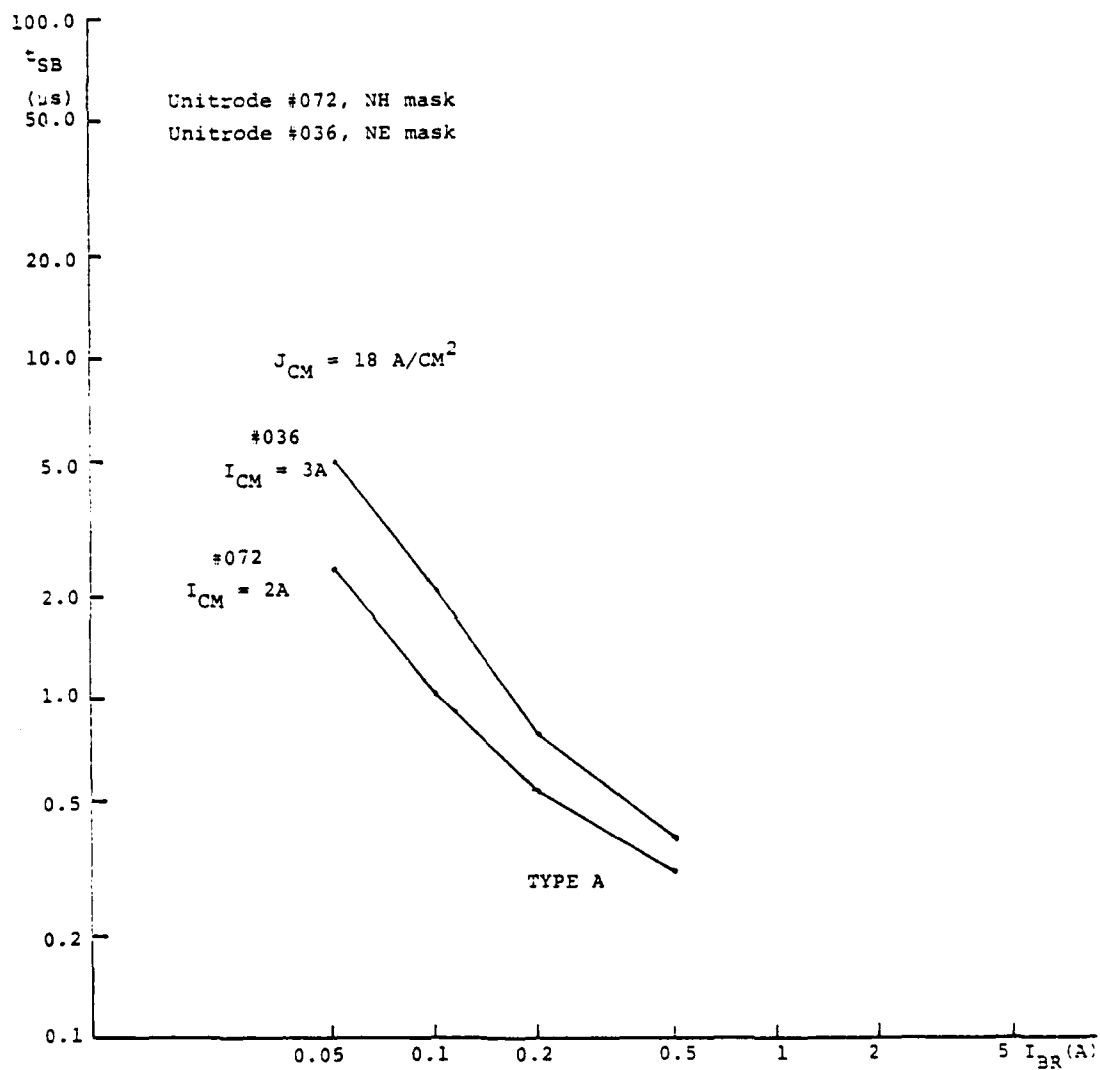


Figure 31. Time to second breakdown vs. reverse base current for collector current density, $J_{CM}' = 18 \text{ A/cm}^2$ in two unitrode devices.

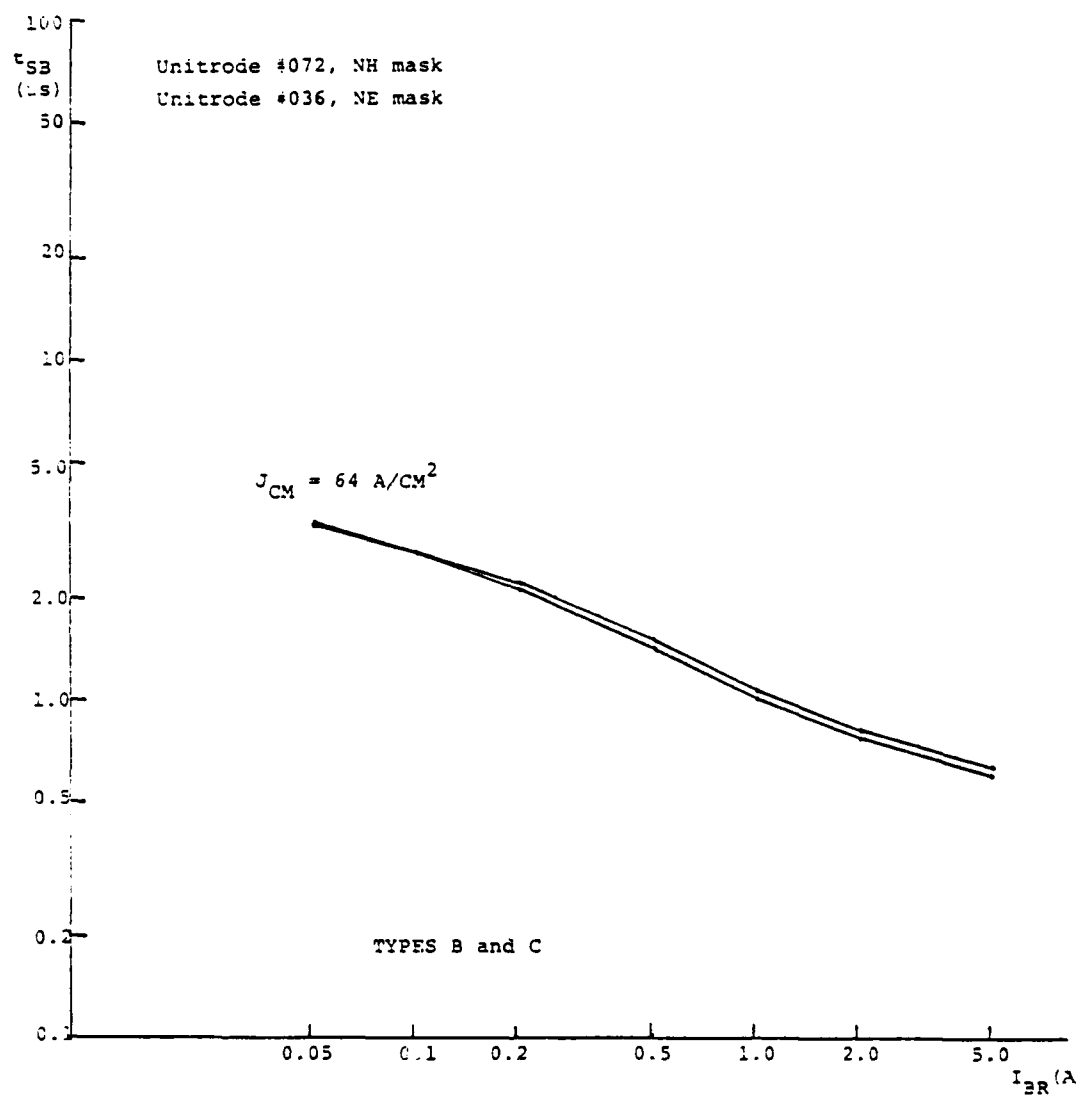


Figure 32. Time to second breakdown vs. reverse base current for collector current density, J_{CM} , $= 64 \text{ A/cm}^2$ in two Unitrode devices.

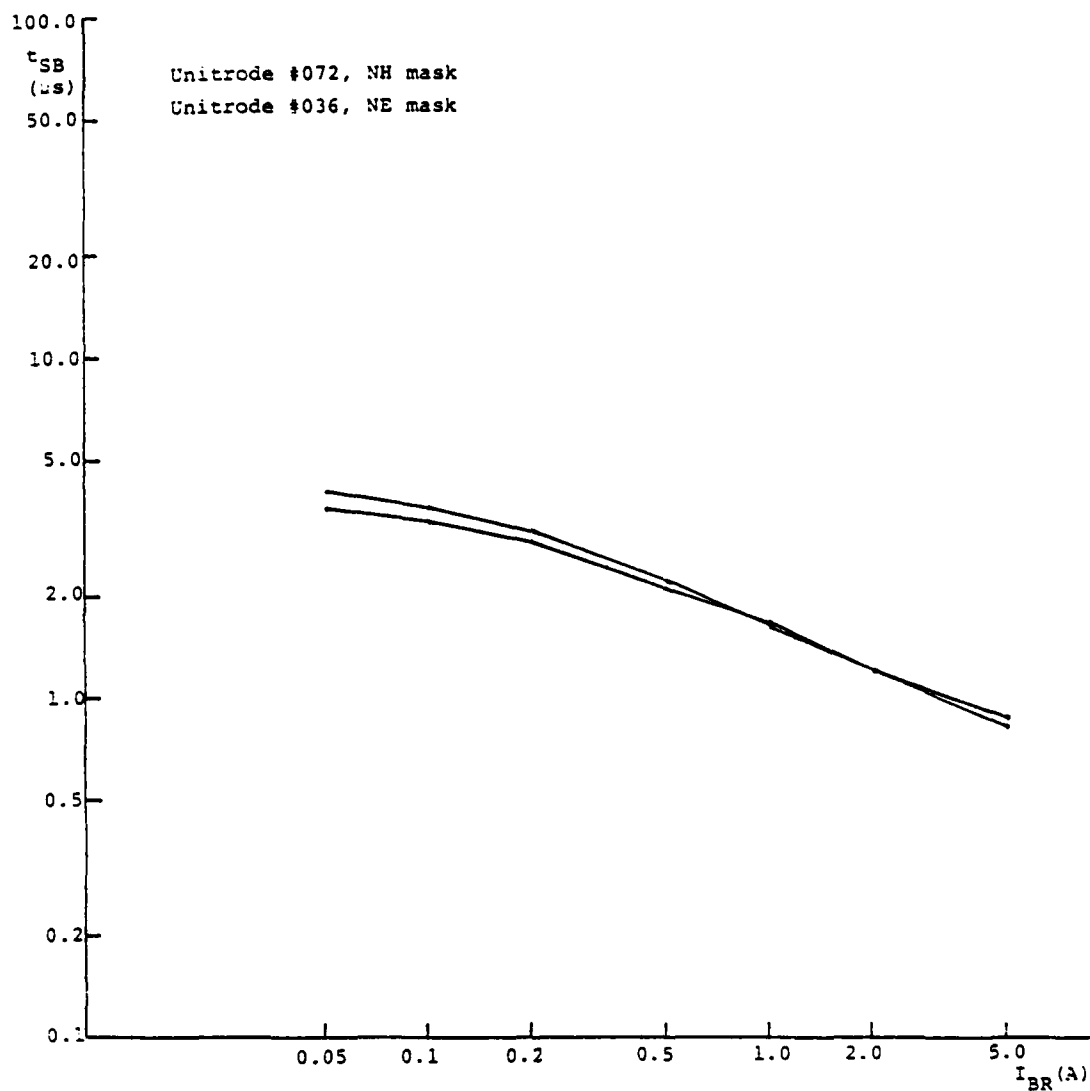


Figure 33. Time to second breakdown vs. reverse base current for collector current density, $J_{CM} = 82$ A/cm² in two Unitrode devices.

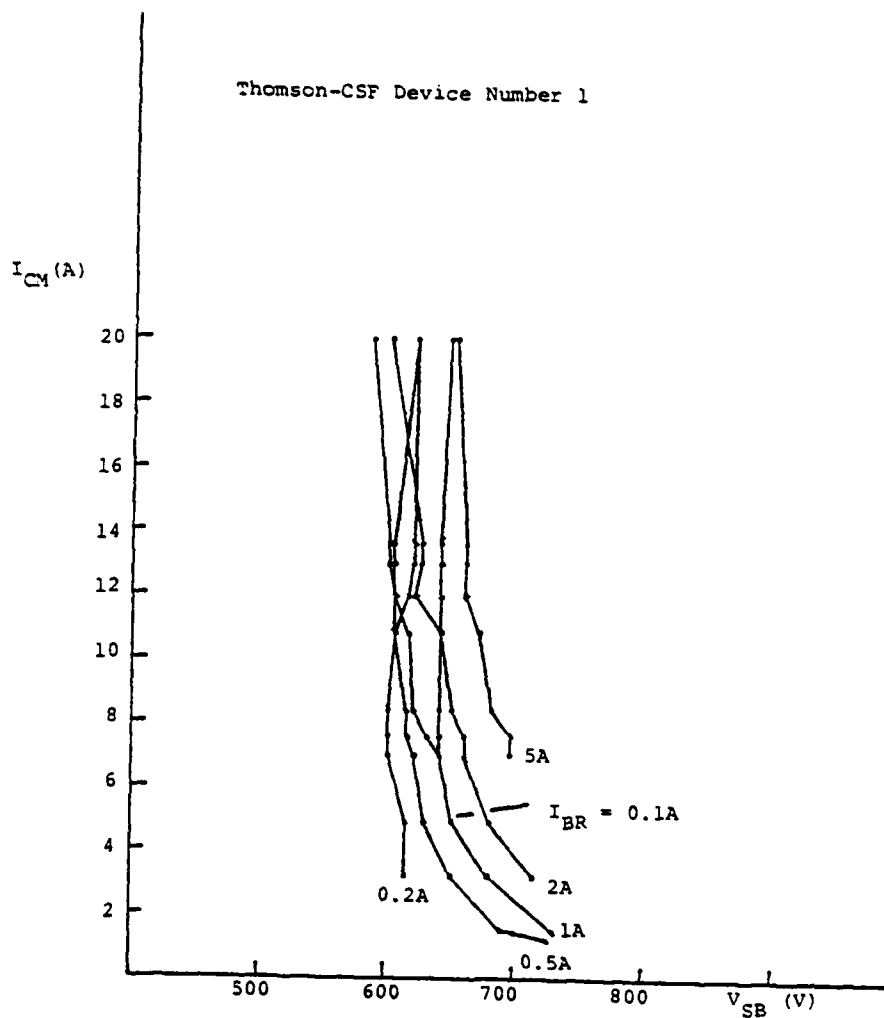


Figure 34. Maximum collector current (at turn-off) vs. second breakdown voltage.

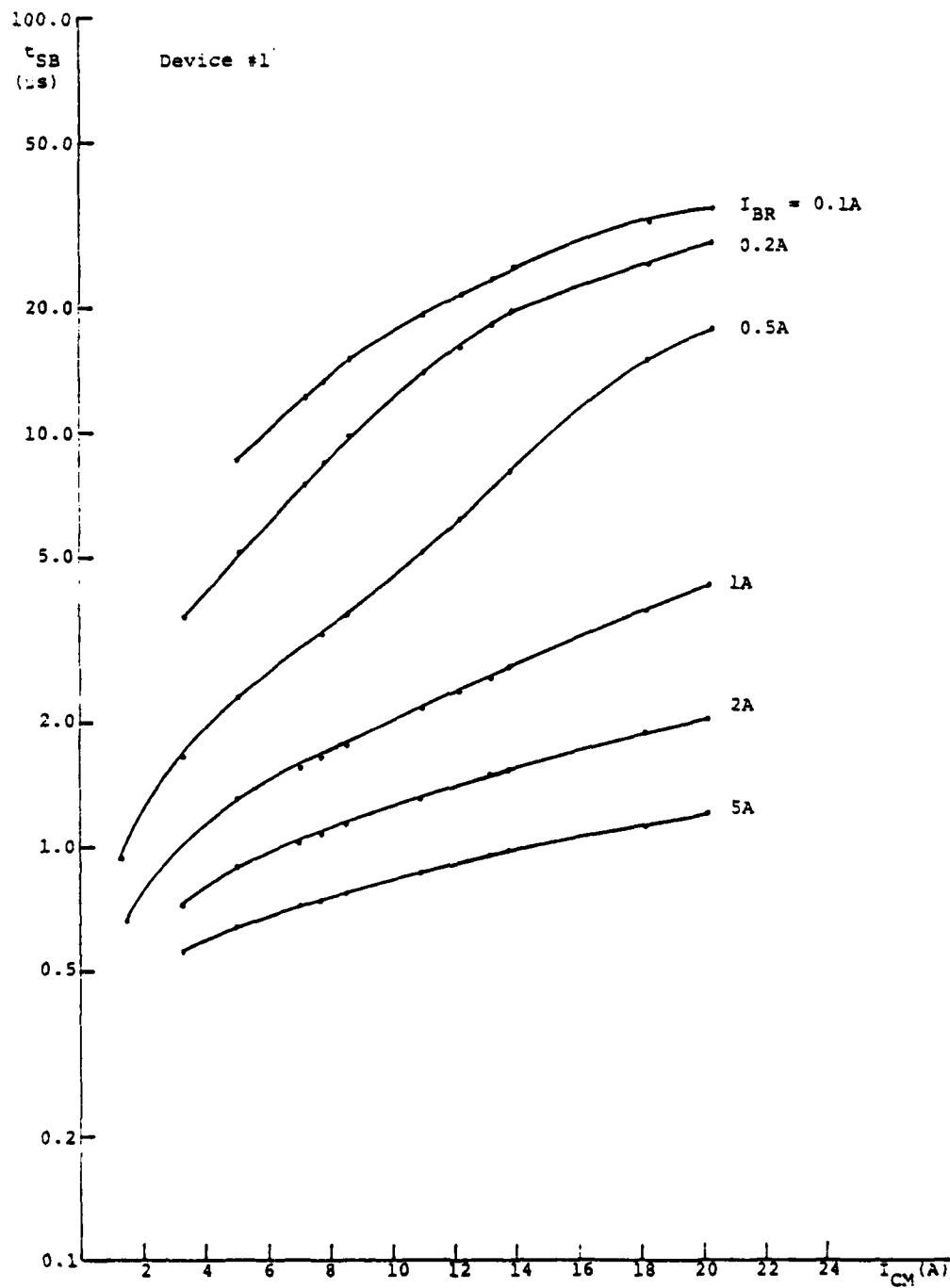


Figure 35. Time to second breakdown vs. maximum collector current (at turn-off).

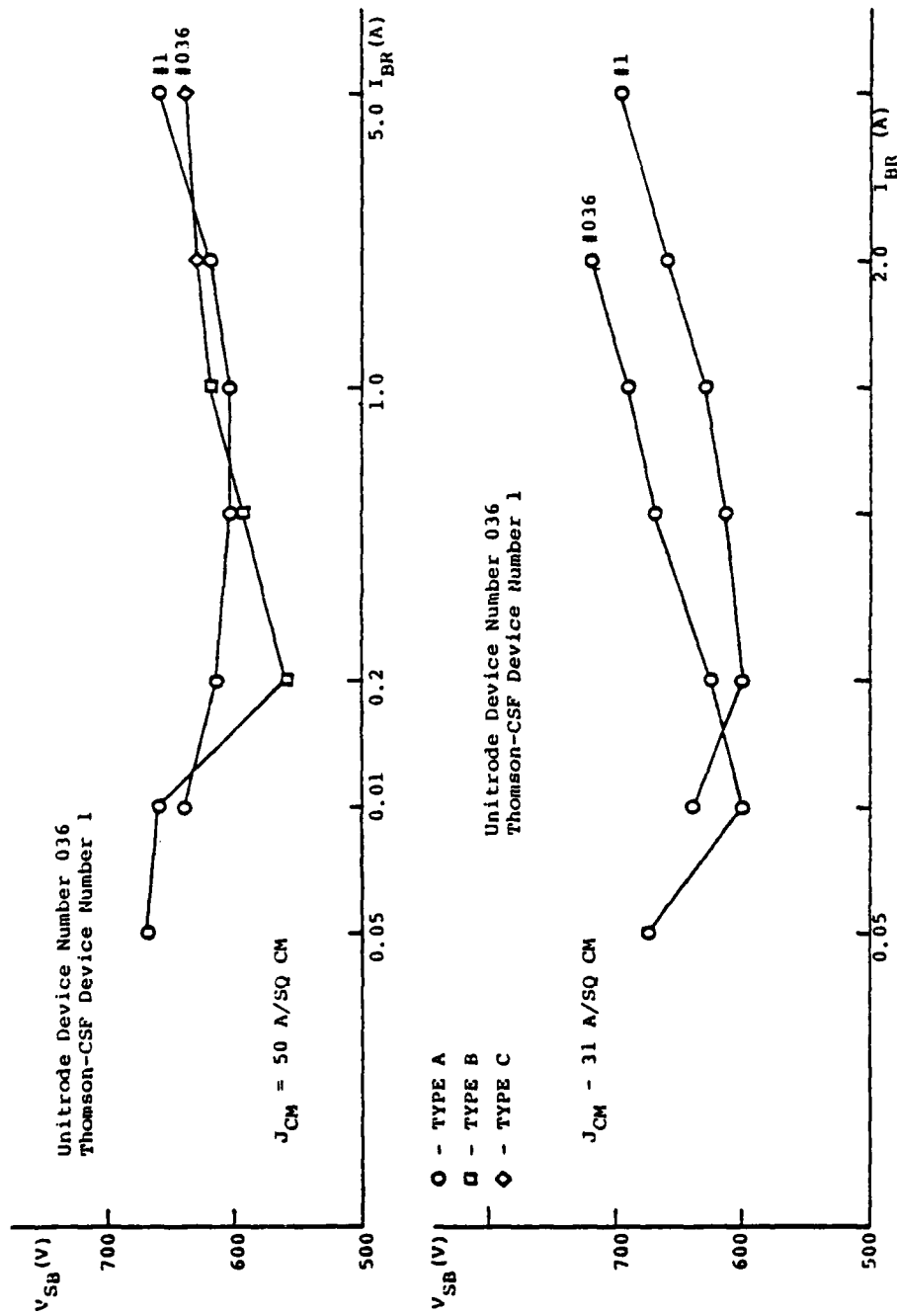


Figure 36. V_{SB} vs. I_{BR} for two collector current densities, $J_{CM} = 31 \text{ A/cm}^2$ and 50 A/cm^2 , for one Unitrode and one Thomson-CSF device.

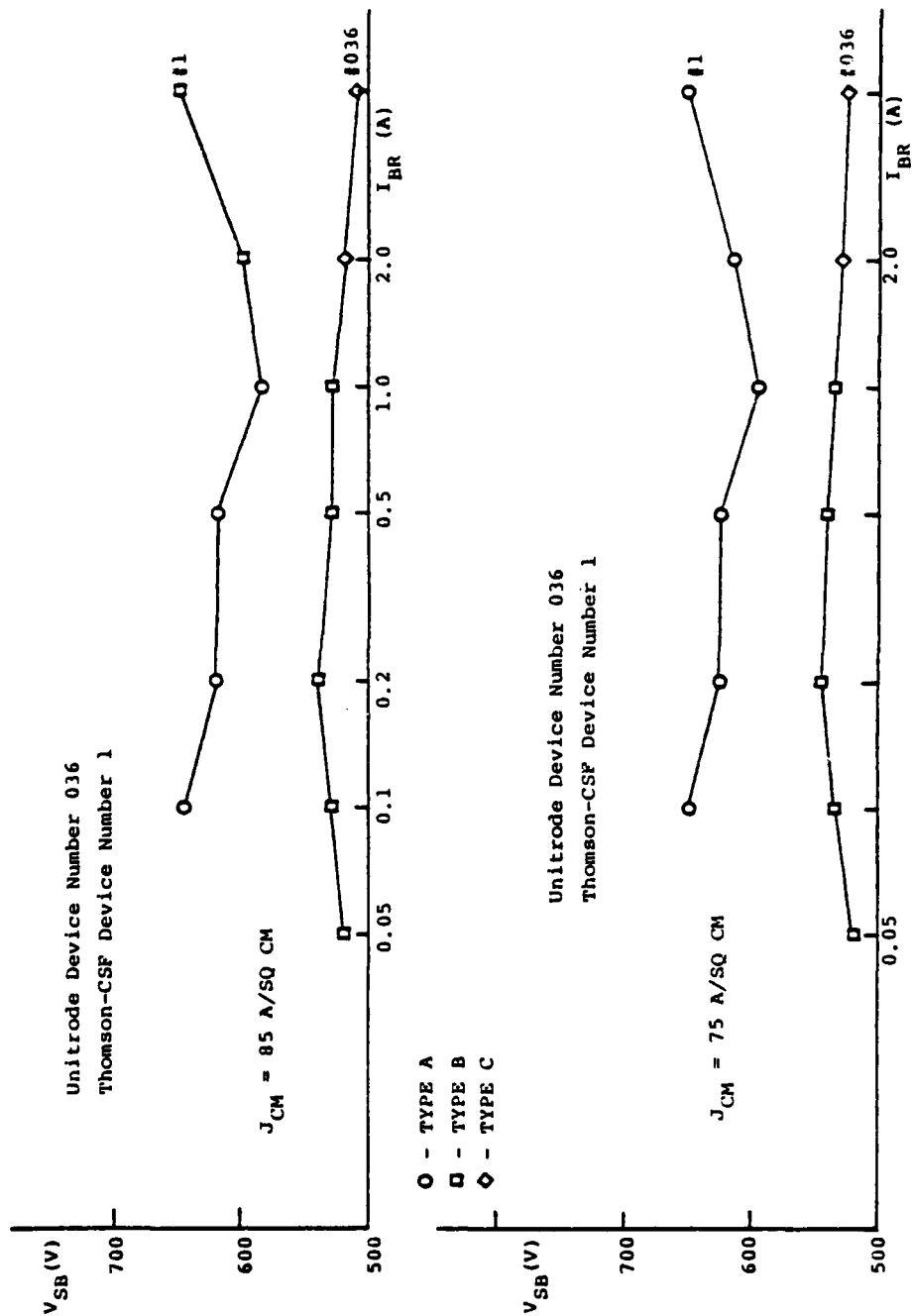


Figure 37. V_{SB} vs. I_{BR} for two collector current densities, $J_{CM} = 75 \text{ A/cm}^2$ and 85 A/cm^2 , for one Unitrode and one Thomson-CSF device.

IV. CONCLUSIONS

These results indicate that, even in a single device, different primary mechanisms may be responsible for reverse bias second breakdown in different operating regions of a transistor. Types A, B, and C have been observed in eleven samples of a single device type furnished by Unitrode; and Types A and B in three samples of a similarly rated device furnished by Thomson-CSF. These observations have been reproducible at constant conditions of maximum collector current and reverse base drive, so that degradation of a device cannot be used to explain the changes in the type of second breakdown observed in the different operating regions. Although a critical temperature cannot at this time be completely excluded as a primary mechanism, it is clear from Figure 30 that adiabatic heating is not an acceptable model. Adiabatic heating to a critical temperature, followed by second breakdown, would require sharp peaking of the curve at some energy, which does not occur. This mechanism does not appear to be important in any of the types of second breakdown observed, and on the basis of existing theory, no thermal mechanism at all is required to explain the Type C results.

However, suggestive as these results are, additional data are required. First, more Type C data must be obtained to complete the energy argument; the reverse base drive available for this work was found to be too low to obtain sufficient Type C breakdowns. Next, a higher forward base drive is required to assure that all devices tested can be driven well into saturation, inasmuch as it is possible that Type C breakdown is a saturation effect. There should be more comparisons among similarly rated power switching devices from different manufacturers; also, single-diffused devices, which theoretically, should not exhibit Type C behavior, should be examined. Finally, measurements at different temperatures, to determine if and how the types are temperature dependent, should be performed.

LIST OF REFERENCES

1. C. G. Thornton and C. D. Simmons, "A new high current mode of transistor operation," IRE Trans. Electron Devices, Vol. ED-5, pp. 6-10, January 1958.
2. G. M. Ford, "Collector to emitter breakdown related to thermal runaway in homogeneous base germanium power transistors," Solid-State Design, Vol. 4, pp. 29-36, June 1963.
3. S. R. Morrison and R. Billette, "Common emitter breakdown," IEEE Trans. Electron Devices, Vol. ED-10, pp. 351-356, November 1963.
4. B. A. Beatty, S. Krishna and M. S. Adler, "Second breakdown in power transistors due to avalanche injection," IEEE Trans. Electron Devices, Vol. ED-23, pp. 851-857, August 1976.
5. P. L. Hower and V. G. Reddi, "Avalanche injection and second breakdown in transistors," IEEE Trans. Electron Devices, Vol. ED-17, pp. 320-335, April 1970.
6. D. W. Berning, Semiconductor Measurement Technology: "A reverse-bias safe operating area transistor tester," NBS special publication 400-54, April 1979.
7. S. R. Morrison and R. Billette, "Common emitter breakdown," IEEE Trans. Electron Devices, Vol. ED-10, pp. 351-356, November 1963.
8. P. L. Hower, "High-field phenomena and failure mechanisms in bipolar transistors," Electrical Overstress Symposium, San Diego, 1980.
9. D. L. Blackburn and D. W. Berning, "Some effects of base current on transistor switching and reverse-bias second breakdown," IEDM Technical Digest, 1978, pp. 671-675.
10. S. K. Ghandhi, Semiconductor Power Devices; John Wiley and Sons, New York, New York, 1977, pp. 174-175.
11. S. K. Ghandhi, The Theory and Practice of Microelectronics; John Wiley and Sons, New York, New York, 1968, pp. 353-355.
12. P. L. Hower, "A model for turn-off in bipolar transistors," IEDM Technical Digest, 1980, pp. 289-292.
13. P. L. Hower, Unitrode, private conversation.

ATE
MED
8